GigaDevice Semiconductor Inc.

GD32A503xx
Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 1.9

(Oct. 2024)

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1. General description

The GD32A503xx device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The processor is based on the ARMv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32A503xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at up to 100 MHz frequency with Flash accesses 0~3 waiting time to obtain maximum efficiency. It provides up to 384 KB on-chip Flash memory and up to 48 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer two 12-bit ADCs, one DAC, one comparator, up to one general 16-bit timer, two basic timers, four PWM advanced timers, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs, three USARTs, one I2S, and two CANs. Additional peripherals as trigger selection controller (TRIGSEL), multi-function communication interface (MFCOM), DMA request multiplexer (DMAMUX) are included.

The device operates from a 2.7 to 5.5 V power supply and available in –40 to +125 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32A503xx devices suitable for a wide range of applications, especially in areas such as BCM, HVAC, BMS, OBC(on-board charger), automotive radar, automotive vision, DC-DC, automobile instrument, IVI(in-vehicle infotatinment) and so on.

2. Device overview

2.1. Device information

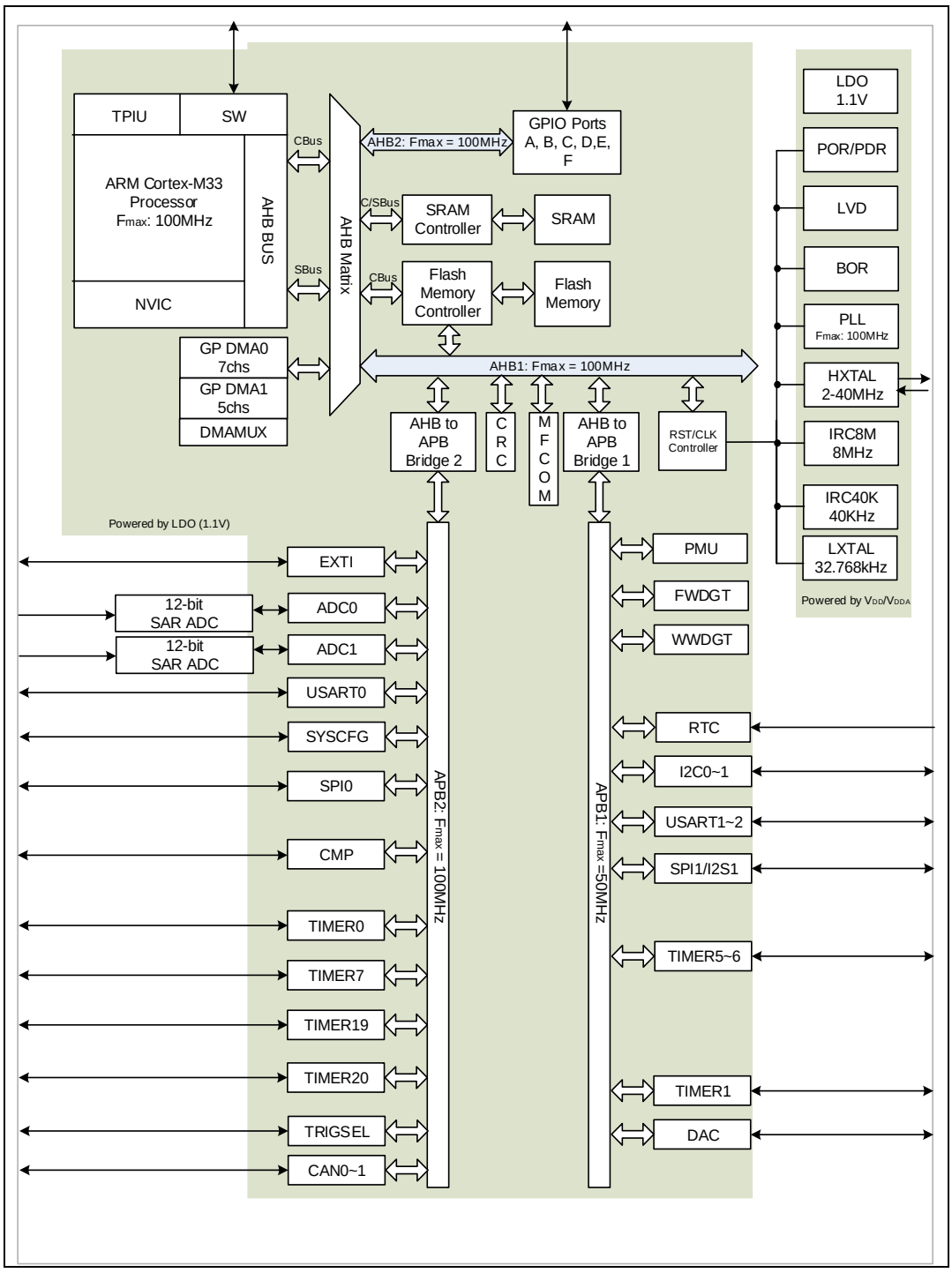
Table 2-1. GD32A503xx devices features and peripheral list

Part Number		GD32A503xx									
		KB	KC	CB	CC	RB	RC	RD	VB	VC	VD
Safety-ISO26262		ASIL-B READY									
FLASH (KB)		128	256	128	256	128	256	384	128	256	384
SRAM (KB)		24	32	24	32	24	32	48	24	32	48
Data Flash & EEPROM backup (KB)		32	64	32	64	32	64	64	32	64	64
EEPROM (KB)		2	4	2	4	2	4	4	2	4	4
Timers	General timer(16-bit)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)
	Advanced timer(16-bit)	3 (0,7,19)	4 (0,7,19,20)	3 (0,7,19)	4 (0,7,19,20)	3 (0,7,19)	4 (0,7,19,20)	4 (0,7,19,20)	4 (0,7,19,20)	4 (0,7,19,20)	4 (0,7,19,20)
	SysTick	1	1	1	1	1	1	1	1	1	1
	Basic timer(16-bit)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)	2 (5-6)
	Watchdog	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	1 (0)	1 (0)	2 (0-1)	2 (0-1)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	I2C	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SPI/I2S	1/0 (0)/none	1/0 (0)/none	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)
	MFCOM	1	1	1	1	1	1	1	1	1	1
	CAN	1×FD (0)	1×FD (0)	2×FD (0-1)	2×FD (0-1)	2×FD (0-1)	2×FD (0-1)	2×FD (0-1)	2×FD (0-1)	2×FD (0-1)	2×FD (0-1)
GPIO		27	27	42	42	57	57	57	88	88	88
DAC		1	1	1	1	1	1	1	1	1	1
CMP		1	1	1	1	1	1	1	1	1	1
ADC	Units	2	2	2	2	2	2	2	2	2	2
	Channels	12	12	20	20	27	27	27	32	32	32

Package	QFN32	LQFP48	LQFP64	LQFP100

2.2. Block diagram

Figure 2-1. GD32A503xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32A503Vx LQFP100 pinouts

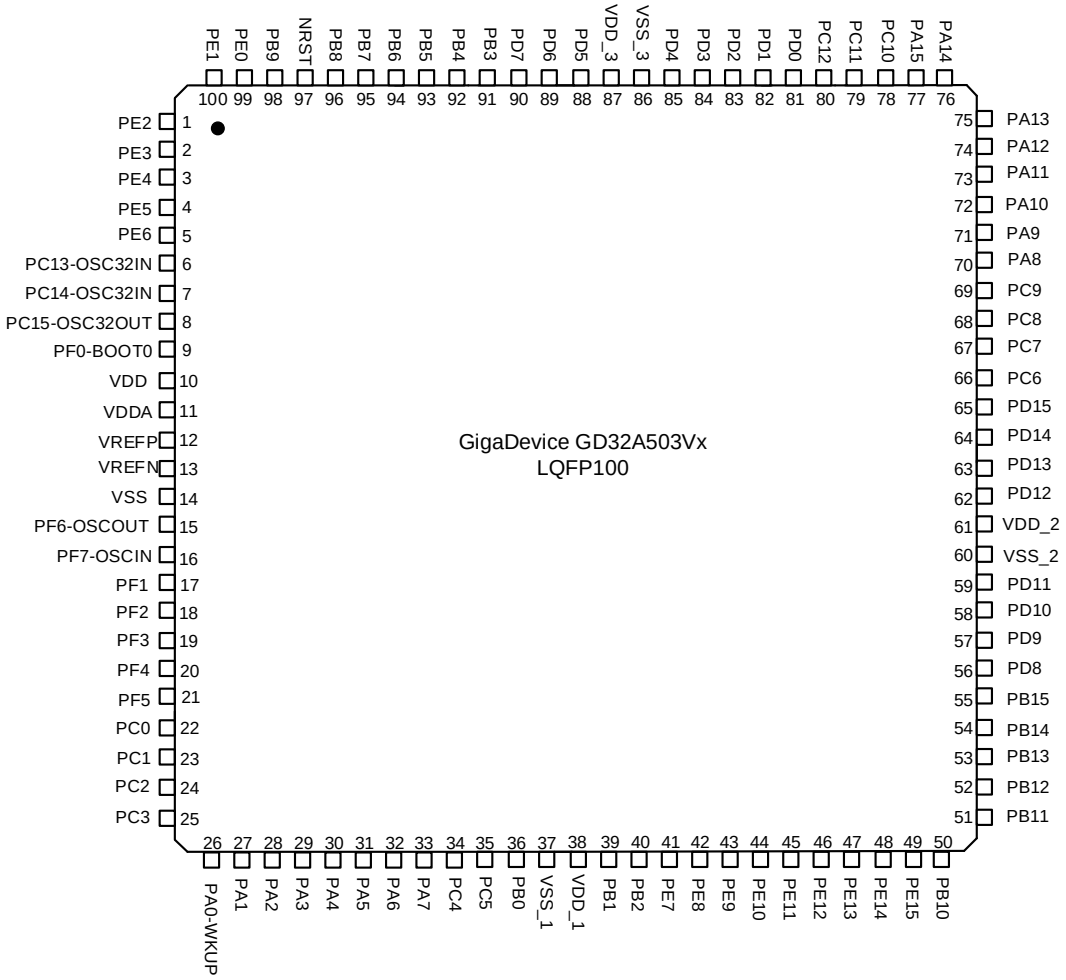


Figure 2-3. GD32A503Rx LQFP64 pinouts

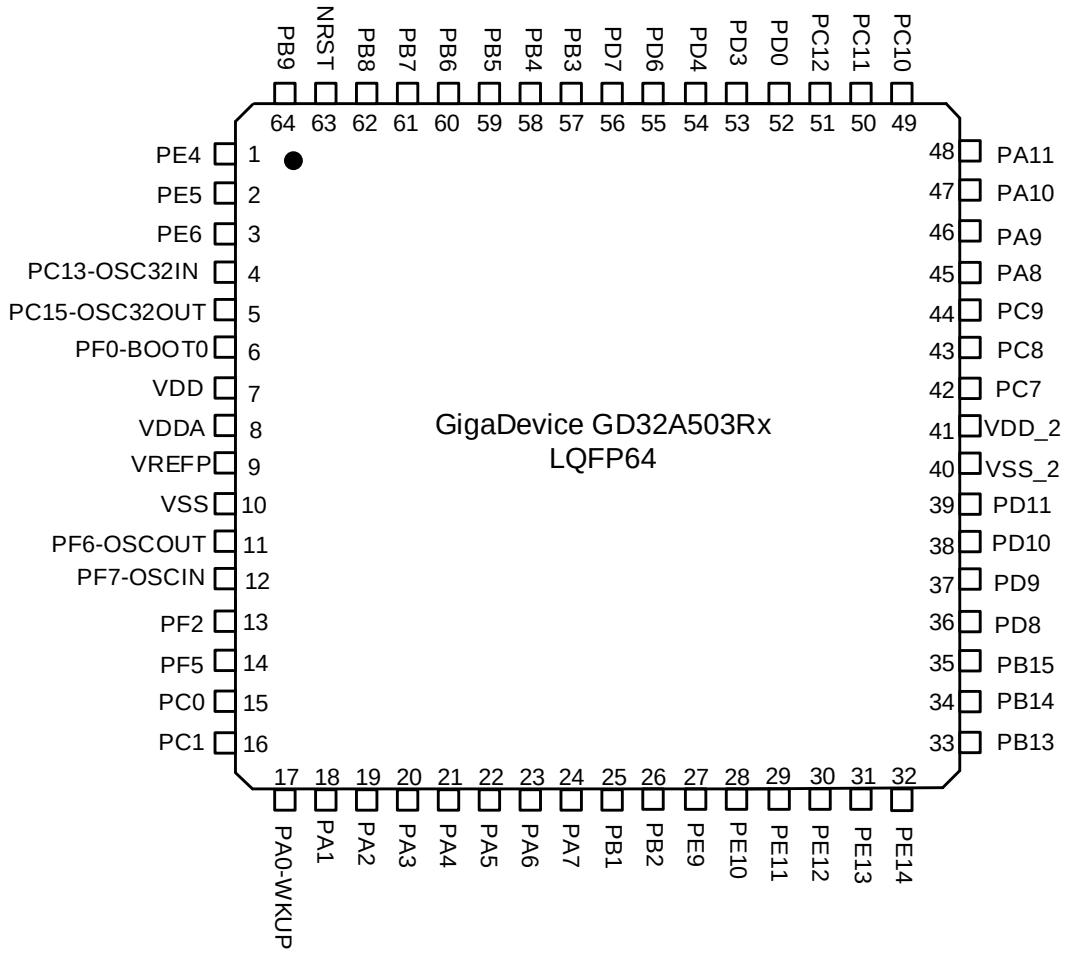


Figure 2-4. GD32A503Cx LQFP48 pinouts

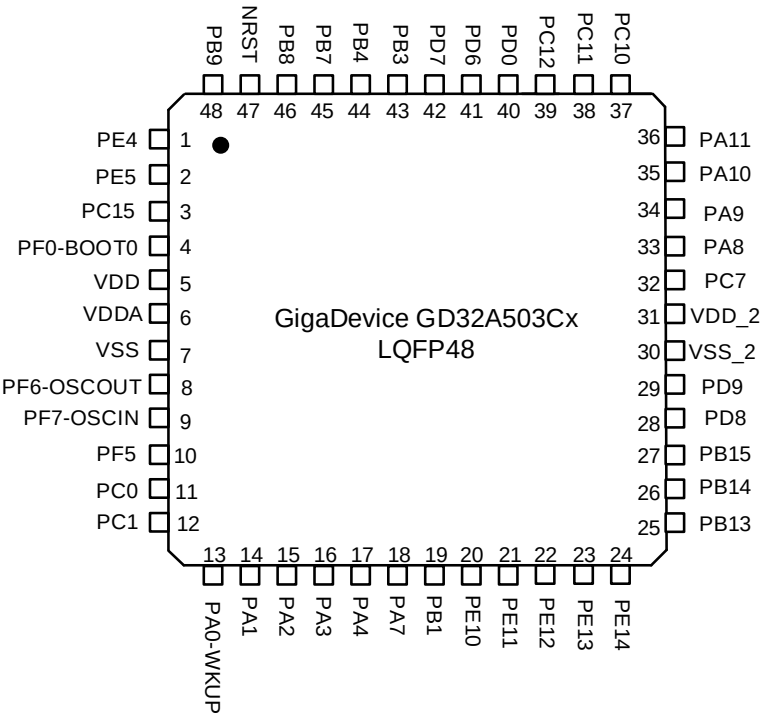
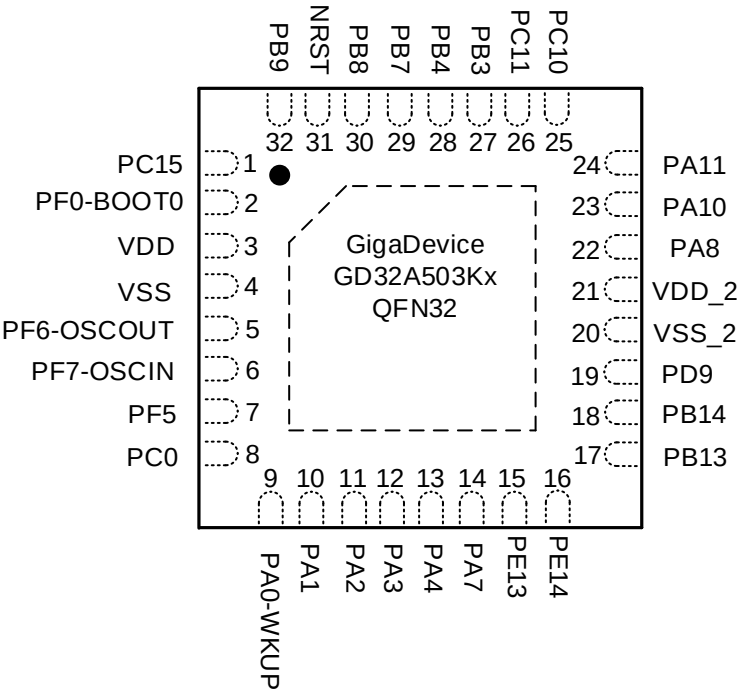


Figure 2-5. GD32A503Kx QFN32 pinouts



2.4. Memory map

Table 2-2. GD32A503xx memory map

Pre-defined Regions	Bus	Address	Peripherals
		0xE004 4400 - 0xE00F FFFF	Cortex M33 internal peripherals
		0xE004 4000 – 0xE004 43FF	DBG
		0xE000 0000 – 0xE004 3FFF	Cortex M33 internal peripherals
External RAM		0x6000 0000 - 0x9FFF FFFF	Reserved
Peripheral	AHB1	0x5000 0000 - 0x5FFF FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	GPIOE
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4003 8C00 - 0x47FF FFFF	Reserved
		0x4003 8400 - 0x4003 8BFF	MFCOM
		0x4002 3400 - 0x4003 83FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
	APB2	0x4001 C000 - 0x4001 FFFF	Reserved
		0x4001 B000 - 0x4001 BFFF	CAN1
		0x4001 A000 - 0x4001 AFFF	CAN0
		0x4001 8800 - 0x4001 9FFF	Reserved
		0x4001 8400 - 0x4001 87FF	TRIGSEL
		0x4001 8000 - 0x4001 83FF	Reserved
		0x4001 7C00 - 0x4001 7FFF	CMP
		0x4001 5800 - 0x4001 7BFF	Reserved
		0x4001 5400 - 0x4001 57FF	TIMER20

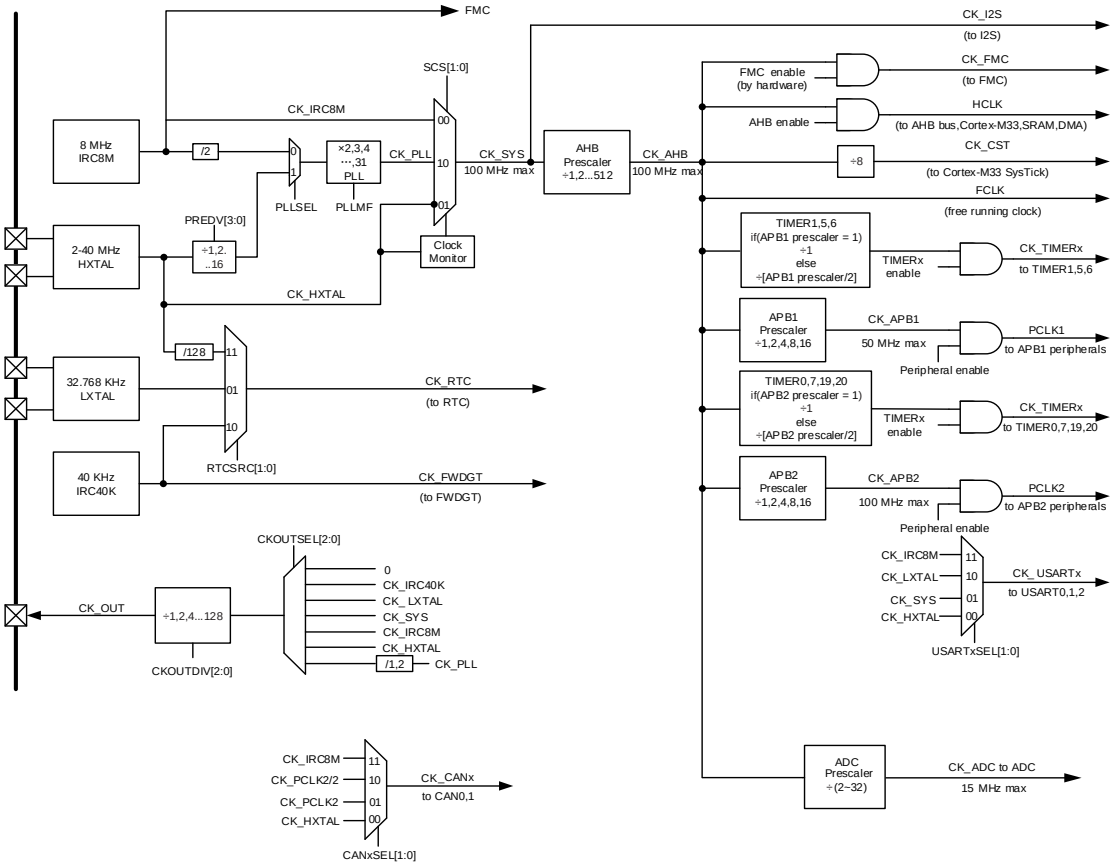
Pre-defined Regions	Bus	Address	Peripherals
		0x4001 5000 - 0x4001 53FF	TIMER19
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	Reserved
		0x4001 4000 - 0x4001 43FF	Reserved
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	Reserved
		0x4001 1000 - 0x4001 13FF	Reserved
		0x4001 0C00 - 0x4001 0FFF	Reserved
		0x4001 0800 - 0x4001 0BFF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG
	APB1	0x4000 DC00 - 0x4000 FFFF	Reserved
		0x4000 D800 - 0x4000 DBFF	Reserved
		0x4000 D400 - 0x4000 D7FF	Reserved
		0x4000 D000 - 0x4000 D3FF	Reserved
		0x4000 CC00 - 0x4000 CFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	Reserved
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8800 - 0x4000 BFFF	Reserved
		0x4000 8400 - 0x4000 87FF	Reserved
		0x4000 8000 - 0x4000 83FF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	BKP
		0x4000 6800 - 0x4000 6BFF	Reserved
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	Reserved
		0x4000 4C00 - 0x4000 4FFF	Reserved
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	Reserved
		0x4000 0800 - 0x4000 0BFF	Reserved
		0x4000 0400 - 0x4000 07FF	Reserved
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2000 D000 - 0x3FFF FFFF	Reserved
		0x2000 C000 - 0x2000 CFFF	Shared SRAM(4KB)
		0x2000 5000 - 0x2000 BFFF	SRAM(48KB)
		0x2000 2000 - 0x2000 4FFF	
		0x2000 1000 - 0x2000 1FFF	
		0x2000 0000 - 0x2000 0FFF	
Code		0x1FFF FC4 - 0x1FFF FFFF	Reserved
		0x1FFF FC00 - 0x1FFF FC0F	Reserved
		0x1FFF F818 - 0x1FFF BFFF	Reserved
		0x1FFF F800 - 0x1FFF F817	Option Bytes (24B)
		0x1FFF B000 - 0x1FFF F7FF	System memory(18KB)
		0x1FFF 7400 - 0x1FFF AFFF	Reserved
		0x1FFF 7000 - 0x1FFF 73FF	OTP(1KB)
		0x0A00 D000 - 0x1FFF 6FFF	Reserved
		0x0A00 C000 - 0x0A00 CFFF	Shared SRAM(4KB)
		0x0A00 0000 - 0x0A00 BFFF	SRAM(48KB)

Pre-defined Regions	Bus	Address	Peripherals
		0x08C0 1000 - 0x09FF FFFF	Reserved
		0x08C0 0000 - 0x08C0 0FFF	EEPROM(4KB)
		0x0881 0000 - 0x08BF FFFF	Reserved
		0x0880 0000 - 0x0880 FFFF	DFlash(64KB)
		0x0808 0000 - 0x0871 FFFF	Reserved
		0x0806 0000 - 0x0807 FFFF	Reserved
		0x0802 0000 - 0x0805 FFFF	Main Flash memory
		0x0801 0000 - 0x0801 FFFF	
		0x0800 0000 - 0x0800 FFFF	
		0x0006 0000 - 0x07FF FFFF	Reserved
		0x0002 0000 - 0x0005 FFFF	Aliased to Flash or system memory
		0x0001 0000 - 0x0001 FFFF	
		0x0000 0000 - 0x0000 FFFF	

2.5. Clock tree

Figure 2-6. GD32A503xx clock tree



Note:

If the APB prescaler is 1, the timer clock frequencies are set to AHB frequency divide by 1. Otherwise, they are set to the AHB frequency divide by half of APB prescaler.

Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillator

IRC40K: Internal 40K RC oscillator

2.6. Pin definitions

2.6.1. GD32A503Vx LQFP100 pin definitions

Table 2-3. GD32A503Vx LQFP100 pin definitions

GD32A503Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O		Default: PE2 Alternate: TIMER19_MCH3, USART1_RTS, USART1_DE, MFCOM_D3, TRIGSEL_OUT7, EVENTOUT
PE3	2	I/O		Default: PE3 Alternate: TIMER19_CH3, USART1_CTS, MFCOM_D2, TRIGSEL_OUT6, EVENTOUT
PE4	3	I/O		Default: PE4 Alternate: TIMER0_MCH1, TIMER19_MCH0, SPI1_MISO, MFCOM_D1, TRIGSEL_OUT2, EVENTOUT
PE5	4	I/O		Default: PE5 Alternate: TIMER0_CH1, TIMER19_CH0, SPI1_SCK, I2S1_CK, MFCOM_D0, TRIGSEL_OUT1, EVENTOUT
PE6	5	I/O		Default: PE6 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER19_MCH2, I2S1_MCK, MFCOM_D5, TRIGSEL_OUT5, EVENTOUT
PC13-OSC32IN	6	I/O		Default: PC13 Alternate: CK_OUT, TIMER19_CH2, MFCOM_D4, TRIGSEL_OUT4, EVENTOUT Additional: WKUP1, OSC32IN
PC14-OSC32IN	7	I/O		Default: PC14 Alternate: TIMER19_BRKIN0, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	8	I/O		Default: PC15 Alternate: TIMER_ETI2(3), TIMER19_MCH1, TIMER19_CH1, CAN0_TX, MFCOM_D7, EVENTOUT Additional: OSC32OUT
PF0-BOOT0	9	I/O		Default: PF0(4) Alternate: TIMER19_CH1, CAN0_RX, MFCOM_D6, EVENTOUT Additional: BOOT0
VDD	10	P		Default: VDD
VDDA	11	P		Default: VDDA
VREFP	12	P		Default: VREFP

GD32A503Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VREFN	13	P		Default: VREFN
VSS	14	P		Default: VSS
PF6-OSCOUT	15	I/O		Default: PF6 Alternate: I2C0_SCL, EVENTOUT Additional: OSCOUT
PF7-OSCIN	16	I/O		Default: PF7 Alternate: I2C0_SDA, EVENTOUT Additional: OSCIN
PF1	17	I/O		Default: PF1 Alternate: TIMER0_BRKIN1, TIMER19_BRKIN1, EVENTOUT
PF2	18	I/O		Default: PF2 Alternate: TIMER0_BRKIN0, TIMER19_BRKIN0, USART2_RTS, USART2_DE, TRIGSEL_IN6, CMP_OUT, EVENTOUT
PF3	19	I/O		Default: PF3 Alternate: TIMER0_BRKIN3, USART2_TX, EVENTOUT
PF4	20	I/O		Default: PF4 Alternate: TIMER0_BRKIN2, USART2_RX, EVENTOUT
PF5	21	I/O		Default: PF5 Alternate: TIMER0_MCH0, SPI0_MISO, USART1_CTS, EVENTOUT
PC0	22	I/O		Default: PC0 Alternate: TIMER0_CH0, SPI0_SCK, EVENTOUT
PC1	23	I/O		Default: PC1 Alternate: TIMER0_MCH3, USART2_CTS, EVENTOUT
PC2	24	I/O		Default: PC2 Alternate: CK_OUT, TIMER19_MCH2, USART1_TX, EVENTOUT
PC3	25	I/O		Default: PC3 Alternate: TIMER19_CH2, USART1_RX, EVENTOUT
PA0-WKUP	26	I/O		Default: PA0 Alternate: TIMER0_CH3, EVENTOUT Additional: CMP_IM_IP3, WKUP0
PA1	27	I/O		Default: PA1 Alternate: CK_OUT, TIMER0_MCH2, SPI0_NSS, TRIGSEL_IN0, EVENTOUT
PA2	28	I/O		Default: PA2 Alternate: TIMER0_CH2, SPI0_MOSI, TRIGSEL_IN1, EVENTOUT
PA3	29	I/O		Default: PA3

GD32A503Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER0_MCH1, USART0_TX, CAN0_TX, TIMER1_CH3, EVENTOUT Additional: ADC0_IN11, CMP_IM_IP4
PA4	30	I/O		Default: PA4 Alternate: TIMER0_CH1, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN10, CMP_IM_IP5
PA5	31	I/O		Default: PA5 Alternate: TIMER19_BRKIN3, USART2_TX, EVENTOUT Additional: CMP_IM_IP6
PA6	32	I/O		Default: PA6 Alternate: TIMER19_BRKIN2, USART2_RX, EVENTOUT Additional: CMP_IM_IP7
PA7	33	I/O		Default: PA7 Alternate: TIMER19_MCH1, TIMER1_CH1, TIMER19_BRKIN1, TRIGSEL_IN7, EVENTOUT, USART2_CK Additional: DAC_OUT
PC4	34	I/O		Default: PC4 Alternate: TIMER19_CH1, USART2_RTS, USART2_DE, EVENTOUT
PC5	35	I/O		Default: PC5 Alternate: TIMER19_MCH0, TIMER19_CH0, USART2_CTS, EVENTOUT
PB0	36	I/O		Default: PB0 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT
VSS_1	37	P		Default: VSS_1
VDD_1	38	P		Default: VDD_1
PB1	39	I/O		Default: PB1 Alternate: TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: ADC0_IN9(5)
PB2	40	I/O		Default: PB2 Alternate: TIMER0_CH0, TIMER7_CH3, EVENTOUT Additional: ADC0_IN8(5)
PE7	41	I/O		Default: PE7 Alternate: TIMER7_MCH2, TIMER19_BRKIN3, MFCOM_D0, EVENTOUT
PE8	42	I/O		Default: PE8 Alternate: TIMER7_CH2, TIMER19_BRKIN2, MFCOM_D1, EVENTOUT
PE9	43	I/O		Default: PE9 Alternate: TIMER7_BRKIN3, EVENTOUT

GD32A503Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC0_IN15
PE10	44	I/O		Default: PE10 Alternate: TIMER7_BRKIN2, EVENTOUT, I2C1_SCL Additional: ADC0_IN14
PE11	45	I/O		Default: PE11 Alternate: TIMER7_MCH1, TRIGSEL_IN8, EVENTOUT, I2C1_SDA Additional: ADC0_IN13
PE12	46	I/O		Default: PE12 Alternate: TIMER7_CH1, TRIGSEL_IN9, EVENTOUT, I2C1_SMBA Additional: ADC0_IN12
PE13	47	I/O		Default: PE13 Alternate: TIMER7_MCH0, TIMER7_CH0, SPI0_MISO, TRIGSEL_IN2, EVENTOUT Additional: ADC0_IN7
PE14	48	I/O		Default: PE14 Alternate: TIMER7_CH0, TIMER7_CH1, SPI0_SCK, TRIGSEL_IN3, EVENTOUT Additional: ADC0_IN6
PE15	49	I/O		Default: PE15 Alternate: TIMER20_MCH3, TIMER19_MCH3, SPI0_IO2, USART2_RTS, USART2_DE, EVENTOUT
PB10	50	I/O		Default: PB10 Alternate: TIEMR20_CH3, TIMER19_CH3, SPI0_IO3, USART2_CTS, EVENTOUT
PB11	51	I/O		Default: PB11 Alternate: TIMER20_MCH2, TRIGSEL_IN10, TIMER1_CH3, EVENTOUT
PB12	52	I/O		Default: PB12 Alternate: TIMER20_CH2, TRIGSEL_IN11, EVENTOUT
PB13	53	I/O		Default: PB13 Alternate: TIMER_ETI0(3), SPI0_MOSI, USART0_TX, CAN0_TX, EVENTOUT Additional: ADC0_IN5, ADC1_IN15(5)
PB14	54	I/O		Default: PB14 Alternate: TIMER1_CH2, SPI0_NSS, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN4, ADC1_IN14(5)
PB15	55	I/O		Default: PB15 Alternate: TIMER7_BRKIN1, USART1_TX, USART0_RTS, USART0_DE, EVENTOUT

GD32A503Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PD8	56	I/O		Default: PD8 Alternate: TIMER7_BRKIN0, USART1_RX, USART0_CTS, EVENTOUT
PD9	57	I/O		Default: PD9 Alternate: TIMER0_BRKIN2, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC0_IN3
PD10	58	I/O		Default: PD10 Alternate: TIMER0_BRKIN1, SPI1_NSS, I2S1_WS, USART1_CTS, EVENTOUT Additional: ADC0_IN2
PD11	59	I/O		Default: PD11 Alternate: TIMER0_MCH3, TIMER20_BRKIN0, EVENTOUT, I2C1_SMBA
VSS_2	60	P		Default: VSS_2
VDD_2	61	P		Default: VDD_2
PD12	62	I/O		Default: PD12 Alternate: TIMER0_CH3, TIMER20_BRKIN0, EVENTOUT
PD13	63	I/O		Default: PD13 Alternate: TIMER0_MCH2, SPI1_NSS, I2S1_WS, EVENTOUT
PD14	64	I/O		Default: PD14 Alternate: TIMER0_CH2, SPI1_MOSI, I2S1_SD, EVENTOUT Additional: ADC1_IN15(5)
PD15	65	I/O		Default: PD15 Alternate: TIMER0_MCH1, SPI1_MISO, EVENTOUT Additional: ADC1_IN14(5)
PC6	66	I/O		Default: PC6 Alternate: TIMER0_CH1, SPI1_SCK, I2S1_CK, EVENTOUT Additional: ADC1_IN9, ADC0_IN9(5)
PC7	67	I/O		Default: PC7 Alternate: TIMER0_MCH0, TIMER20_BRKIN1, I2S1_MCK, EVENTOUT Additional: ADC1_IN8, ADC0_IN8(5)
PC8	68	I/O		Default: PC8 Alternate: TIMER0_CH0, TIMER20_BRKIN2, EVENTOUT Additional: ADC1_IN7
PC9	69	I/O		Default: PC9

GD32A503Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER0_BRKIN3, TIMER20_BRKIN3, EVENTOUT Additional: ADC1_IN6
PA8	70	I/O		Default: PA8 Alternate: TIMER0_BRKIN0, TIMER20_MCH2, SPI1_NSS, I2S1_WS, MFCOM_D7, MFCOM_D5, TRIGSEL_IN4, EVENTOUT Additional: ADC1_IN3, NMI
PA9	71	I/O		Default: PA9 Alternate: TIMER20_CH2, SPI1_MOSI, I2S1_SD, MFCOM_D6, MFCOM_D4, TRIGSEL_IN5, EVENTOUT Additional: ADC1_IN2
PA10	72	I/O		Default: PA10 Alternate: TIMER20_MCH0, I2C0_SCL, USART0_TX, MFCOM_D5, EVENTOUT Additional: ADC1_IN1
PA11	73	I/O		Default: PA11 Alternate: TIMER20_CH0, I2C0_SDA, USART0_RX, MFCOM_D4, EVENTOUT, TRIGSEL_IN13 Additional: ADC1_IN0
PA12	74	I/O		Default: PA12 Alternate: TIMER20_MCH1, I2C0_SMBA, USART0_CK, EVENTOUT
PA13	75	I/O		Default: PA13 Alternate: TIMER20_CH1, I2C0_SDA, EVENTOUT
PA14	76	I/O		Default: PA14 Alternate: TIMER20_MCH0, I2C0_SCL, EVENTOUT
PA15	77	I/O		Default: PA15 Alternate: TIMER20_CH0, EVENTOUT, TRIGSEL_IN12
PC10	78	I/O		Default: PC10 Alternate: TIMER7_MCH0, TIMER7_CH0, I2C0_SDA, USART0_RTS, USART0_DE, MFCOM_D3, TRIGSEL_OUT0, EVENTOUT Additional: ADC0_IN1, CMP_IM_IP1
PC11	79	I/O		Default: PC11 Alternate: TIMER19_MCH0, TIMER19_CH0, I2C0_SCL, USART0_CTS, MFCOM_D2, TRIGSEL_OUT3, EVENTOUT Additional: ADC0_IN0, CMP_IM_IP0
PC12	80	I/O		Default: PC12 Alternate: TIMER20_MCH1, TIMER7_CH0, USART1_TX, CAN1_TX, EVENTOUT

GD32A503Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC1_IN5
PD0	81	I/O		Default: PD0 Alternate: TIMER20_CH1, TIMER7_CH1, USART1_RX, CAN1_RX, EVENTOUT Additional: ADC1_IN4
PD1	82	I/O		Default: PD1 Alternate: TIMER7_MCH1, SPI1_NSS, I2S1_WS, EVENTOUT Additional: ADC1_IN13
PD2	83	I/O		Default: PD2 Alternate: TIMER7_CH1, SPI0_NSS, EVENTOUT Additional: ADC1_IN12
PD3	84	I/O		Default: PD3 Alternate: TIMER20_MCH3, SPI0_NSS, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC1_IN11
PD4	85	I/O		Default: PD4 Alternate: TIMER20_CH3, TIMER1_CH2, SPI0_MOSI, USART1_CTS, EVENTOUT Additional: ADC1_IN10
VSS_3	86	P		Default: VSS_3
VDD_3	87	P		Default: VDD_3
PD5	88	I/O		Default: PD5 Alternate: TIMER0_BRKIN0, TIMER20_BRKIN1, TIMER7_BRKIN0, USART1_CK, EVENTOUT
PD6	89	I/O		Default: PD6 Alternate: TIMER7_MCH3, TIMER19_CH0, CAN1_TX, EVENTOUT, I2C1_SCL
PD7	90	I/O		Default: PD7 Alternate: TIMER7_CH3, TIMER19_CH1, CAN1_RX, EVENTOUT, I2C1_SDA
PB3	91	I/O		Default: NJTRST, PB3 Alternate: TIMER7_MCH2, SPI0_IO2, MFCOM_D1, EVENTOUT
PB4	92	I/O		Default: JTDO, PB4 Alternate: TIMER7_CH2, SPI0_IO3, MFCOM_D0, EVENTOUT
PB5	93	I/O		Default: PB5 Alternate: TIMER7_BRKIN1, I2C0_SMBA, SPI0_MISO, SPI1_NSS, I2S1_WS, EVENTOUT
PB6	94	I/O		Default: PB6

GD32A503Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER7_BRKIN2, TIMER_ETI1(3), SPI0_SCK, SPI1_MOSI, I2S1_SD, EVENTOUT
PB7	95	I/O		Default: JTDI, PB7 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT, I2C1_SCL
PB8	96	I/O		Default: JTCK, SWCLK, PB8 Alternate: TIMER7_CH0, TIMER7_CH1, EVENTOUT, I2C1_SDA Additional: CMP_IM_IP2
NRST	97	I/O		Default: NRST
PB9	98	I/O		Default: JTMS, SWDIO, PB9 Alternate: CMP_OUT, EVENTOUT, I2C1_SMBA Additional: BOOT1
PE0	99	I/O		Default: PE0 Alternate: TIMER20_BRKIN2, TIMER7_BRKIN3, USART2_TX, MFCOM_D7, EVENTOUT
PE1	100	I/O		Default: PE1 Alternate: TIMER20_BRKIN3, USART2_RX, MFCOM_D6, EVENTOUT

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) This function is controlled by SYSCFG_TIMERINSEL register.

(4) This function is controlled by SYSCFG_CFG0 register.

(5) This function is controlled by SYSCFG_CFG1 register.

2.6.2. GD32A503Rx LQFP64 pin definitions

Table 2-4. GD32A503Rx LQFP64 pin definitions

GD32A503Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE4	1	I/O		Default: PE4 Alternate: TIMER0_MCH1, TIMER19_MCH0, SPI1_MISO, MFCOM_D1, TRIGSEL_OUT2, EVENTOUT
PE5	2	I/O		Default: PE5 Alternate: TIMER0_CH1, TIMER19_CH0, SPI1_SCK, I2S1_CK, MFCOM_D0, TRIGSEL_OUT1, EVENTOUT
PE6	3	I/O		Default: PE6 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER19_MCH2, I2S1_MCK, MFCOM_D5, TRIGSEL_OUT5, EVENTOUT
PC13-OSC32IN	4	I/O		Default: PC13 Alternate: CK_OUT, TIMER19_CH2, MFCOM_D4, TRIGSEL_OUT4, EVENTOUT Additional: WKUP1, OSC32IN
PC15-OSC32OUT	5	I/O		Default: PC15 Alternate: TIMER_ETI2(3), TIMER19_MCH1, TIMER19_CH1, CAN0_TX, MFCOM_D7, EVENTOUT Additional: OSC32OUT
PF0-BOOT0	6	I		Default: PF0(4) Alternate: TIMER19_CH1, CAN0_RX, MFCOM_D6, EVENTOUT Additional: BOOT0
VDD	7	P		Default: VDD
VDDA	8	P		Default: VDDA
VREFP	9	P		Default: VREFP
VSS	10	P		Default: VSS
PF6-OSCOUT	11	O		Default: PF6 Alternate: I2C0_SCL, EVENTOUT Additional: OSCOUT
PF7-OSCIN	12	I		Default: PF7 Alternate: I2C0_SDA, EVENTOUT Additional: OSCIN
PF2	13	I/O		Default: PF2 Alternate: TIMER0_BRKIN0, TIMER19_BRKIN0, USART2_RTS, USART2_DE, TRIGSEL_IN6, CMP_OUT, EVENTOUT
PF5	14	I/O		Default: PF5 Alternate: TIMER0_MCH0, SPI0_MISO, USART1_CTS, EVENTOUT

GD32A503Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC0	15	I/O		Default: PC0 Alternate: TIMER0_CH0, SPI0_SCK, EVENTOUT
PC1	16	I/O		Default: PC1 Alternate: TIMER0_MCH3, USART2_CTS, EVENTOUT
PA0-WKUP	17	I/O		Default: PA0 Alternate: TIMER0_CH3, EVENTOUT Additional: CMP_IM_IP3, WKUP0
PA1	18	I/O		Default: PA1 Alternate: CK_OUT, TIMER0_MCH2, SPI0_NSS, TRIGSEL_IN0, EVENTOUT
PA2	19	I/O		Default: PA2 Alternate: TIMER0_CH2, SPI0_MOSI, TRIGSEL_IN1, EVENTOUT
PA3	20	I/O		Default: PA3 Alternate: TIMER0_MCH1, USART0_TX, CAN0_TX, TIMER1_CH3, EVENTOUT Additional: ADC0_IN11, CMP_IM_IP4
PA4	21	I/O		Default: PA4 Alternate: TIMER0_CH1, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN10, CMP_IM_IP5
PA5	22	I/O		Default: PA5 Alternate: TIMER19_BRKIN3, USART2_TX, EVENTOUT Additional: CMP_IM_IP6
PA6	23	I/O		Default: PA6 Alternate: TIMER19_BRKIN2, USART2_RX, EVENTOUT Additional: CMP_IM_IP7
PA7	24	I/O		Default: PA7 Alternate: TIMER19_MCH1, TIMER1_CH1, TIMER19_BRKIN1, TRIGSEL_IN7, EVENTOUT, USART2_CK Additional: DAC_OUT
PB1	25	I/O		Default: PB1 Alternate: TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: ADC0_IN9
PB2	26	I/O		Default: PB2 Alternate: TIMER0_CH0, TIMER7_CH3, EVENTOUT Additional: ADC0_IN8(5)
PE9	27	I/O		Default: PE9 Alternate: TIMER7_BRKIN3, EVENTOUT Additional: ADC0_IN15
PE10	28	I/O		Default: PE10

GD32A503Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER7_BRKIN2, EVENTOUT, I2C1_SCL Additional: ADC0_IN14
PE11	29	I/O		Default: PE11 Alternate: TIMER7_MCH1, TRIGSEL_IN8, EVENTOUT, I2C1_SDA Additional: ADC0_IN13
PE12	30	I/O		Default: PE12 Alternate: TIMER7_CH1, TRIGSEL_IN9, EVENTOUT, I2C1_SMBA Additional: ADC0_IN12
PE13	31	I/O		Default: PE13 Alternate: TIMER7_MCH0, TIMER7_CH0, SPI0_MISO, TRIGSEL_IN2, EVENTOUT Additional: ADC0_IN7
PE14	32	I/O		Default: PE14 Alternate: TIMER7_CH0, TIMER7_CH1, SPI0_SCK, TRIGSEL_IN3, EVENTOUT Additional: ADC0_IN6
PB13	33	I/O		Default: PB13 Alternate: TIMER_ETI0(3), SPI0_MOSI, USART0_TX, CAN0_TX, EVENTOUT Additional: ADC0_IN5, ADC1_IN15(5)
PB14	34	I/O		Default: PB14 Alternate: TIMER1_CH2, SPI0_NSS, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN4, ADC1_IN14(5)
PB15	35	I/O		Default: PB15 Alternate: TIMER7_BRKIN1, USART1_TX, USART0_RTS, USART0_DE, EVENTOUT
PD8	36	I/O		Default: PD8 Alternate: TIMER7_BRKIN0, USART1_RX, USART0_CTS, EVENTOUT
PD9	37	I/O		Default: PD9 Alternate: TIMER0_BRKIN2, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC0_IN3
PD10	38	I/O		Default: PD10 Alternate: TIMER0_BRKIN1, SPI1_NSS, I2S1_WS, USART1_CTS, EVENTOUT Additional: ADC0_IN2
PD11	39	I/O		Default: PD11 Alternate: TIMER0_MCH3, TIMER20_BRKIN0(6),

GD32A503Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT, I2C1_SMBA
VSS_2	40	P		Default: VSS_2
VDD_2	41	P		Default: VDD_2
PC7	42	I/O		Default: PC7 Alternate: TIMER0_MCH0, TIMER20_BRKIN1(6), I2S1_MCK, EVENTOUT Additional: ADC1_IN8, ADC0_IN8(5)
PC8	43	I/O		Default: PC8 Alternate: TIMER0_CH0, TIMER20_BRKIN2(6), EVENTOUT Additional: ADC1_IN7
PC9	44	I/O		Default: PC9 Alternate: TIMER0_BRKIN3, TIMER20_BRKIN3(6), EVENTOUT Additional: ADC1_IN6
PA8	45	I/O		Default: PA8 Alternate: TIMER0_BRKIN0, TIMER20_MCH2(6), SPI1_NSS, I2S1_WS, MFCOM_D7, MFCOM_D5, TRIGSEL_IN4, EVENTOUT Additional: ADC1_IN3, NMI
PA9	46	I/O		Default: PA9 Alternate: TIMER20_CH2(6), SPI1_MOSI, I2S1_SD, MFCOM_D6, MFCOM_D4, TRIGSEL_IN5, EVENTOUT Additional: ADC1_IN2
PA10	47	I/O		Default: PA10 Alternate: TIMER20_MCH0(6), I2C0_SCL, USART0_TX, MFCOM_D5, EVENTOUT Additional: ADC1_IN1
PA11	48	I/O		Default: PA11 Alternate: TIMER20_CH0(6), I2C0_SDA, USART0_RX, MFCOM_D4, EVENTOUT, TRIGSEL_IN13 Additional: ADC1_IN0
PC10	49	I/O		Default: PC10 Alternate: TIMER7_MCH0, TIMER7_CH0, I2C0_SDA, USART0_RTS, USART0_DE, MFCOM_D3, TRIGSEL_OUT0, EVENTOUT Additional: ADC0_IN1, CMP_IM_IP1
PC11	50	I/O		Default: PC11 Alternate: TIMER19_MCH0, TIMER19_CH0, I2C0_SCL, USART0_CTS, MFCOM_D2, TRIGSEL_OUT3, EVENTOUT Additional: ADC0_IN0, CMP_IM_IP0

GD32A503Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC12	51	I/O		Default: PC12 Alternate: TIMER20_MCH1(6), TIMER7_CH0, USART1_TX, CAN1_TX, EVENTOUT Additional: ADC1_IN5
PD0	52	I/O		Default: PD0 Alternate: TIMER20_CH1(6), TIMER7_CH1, USART1_RX, CAN1_RX, EVENTOUT Additional: ADC1_IN4
PD3	53	I/O		Default: PD3 Alternate: TIMER20_MCH3(6), SPI0_NSS, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC1_IN11
PD4	54	I/O		Default: PD4 Alternate: TIMER20_CH3(6), TIMER1_CH2, SPI0_MOSI, USART1_CTS, EVENTOUT Additional: ADC1_IN10
PD6	55	I/O		Default: PD6 Alternate: TIMER7_MCH3, TIMER19_CH0, CAN1_TX, EVENTOUT, I2C1_SCL
PD7	56	I/O		Default: PD7 Alternate: TIMER7_CH3, TIMER19_CH1, CAN1_RX, EVENTOUT, I2C1_SDA
PB3	57	I/O		Default: NJTRST, PB3 Alternate: TIMER7_MCH2, SPI0_IO2, MFCOM_D1, EVENTOUT
PB4	58	I/O		Default: JTDO, PB4 Alternate: TIMER7_CH2, SPI0_IO3, MFCOM_D0, EVENTOUT
PB5	59	I/O		Default: PB5 Alternate: TIMER7_BRKIN1, I2C0_SMBA, SPI0_MISO, SPI1_NSS, I2S1_WS, EVENTOUT
PB6	60	I/O		Default: PB6 Alternate: TIMER7_BRKIN2, TIMER_ETI1(3), SPI0_SCK, SPI1_MOSI, I2S1_SD, EVENTOUT
PB7	61	I/O		Default: JTDI, PB7 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT, I2C1_SCL
PB8	62	I/O		Default: JTCK, SWCLK, PB8 Alternate: TIMER7_CH0, TIMER7_CH1, EVENTOUT, I2C1_SDA Additional: CMP_IM_IP2
NRST	63	I/O		Default: NRST

GD32A503Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB9	64	I/O		Default: JTMS, SWDIO, PB9 Alternate: CMP_OUT, EVENTOUT, I2C1_SMBA Additional: BOOT1

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) This function is controlled by SYSCFG_TIMERINSEL register.

(4) This function is controlled by SYSCFG_CFG0 register.

(5) This function is controlled by SYSCFG_CFG1 register.

(6) Functions are available on GD32A503RC/D devices only.

2.6.3. GD32A503Cx LQFP48 pin definitions

Table 2-5. GD32A503Cx LQFP48 pin definitions

GD32A503Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE4	1	I/O		Default: PE4 Alternate: TIMER0_MCH1, TIMER19_MCH0, SPI1_MISO, MFCOM_D1, TRIGSEL_OUT2, EVENTOUT
PE5	2	I/O		Default: PE5 Alternate: TIMER0_CH1, TIMER19_CH0, SPI1_SCK, I2S1_CK, MFCOM_D0, TRIGSEL_OUT1, EVENTOUT
PC15	3	I/O		Default: PC15 Alternate: TIMER_ETI2(3), TIMER19_MCH1, TIMER19_CH1, CAN0_TX, MFCOM_D7, EVENTOUT
PF0-BOOT0	4	I/O		Default: PF0(4) Alternate: TIMER19_CH1, CAN0_RX, MFCOM_D6, EVENTOUT Additional: BOOT0
VDD	5	P		Default: VDD
VDDA	6	P		Default: VDDA
VSS	7	P		Default: VSS
PF6-OSCOUT	8	I/O		Default: PF6 Alternate: I2C0_SCL, EVENTOUT Additional: OSCOUT
PF7-OSCIN	9	I/O		Default: PF7 Alternate: I2C0_SDA, EVENTOUT Additional: OSCIN
PF5	10	I/O		Default: PF5 Alternate: TIMER0_MCH0, SPI0_MISO, USART1_CTS, EVENTOUT
PC0	11	I/O		Default: PC0 Alternate: TIMER0_CH0, SPI0_SCK, EVENTOUT
PC1	12	I/O		Default: PC1 Alternate: TIMER0_MCH3, EVENTOUT
PA0-WKUP	13	I/O		Default: PA0 Alternate: TIMER0_CH3, EVENTOUT Additional: CMP_IM_IP3, WKUP0
PA1	14	I/O		Default: PA1 Alternate: CK_OUT, TIMER0_MCH2, SPI0_NSS, TRIGSEL_IN0, EVENTOUT
PA2	15	I/O		Default: PA2 Alternate: TIMER0_CH2, SPI0_MOSI, TRIGSEL_IN1, EVENTOUT

GD32A503Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA3	16	I/O		Default: PA3 Alternate: TIMER0_MCH1, USART0_TX, CAN0_TX, TIMER1_CH3, EVENTOUT Additional: ADC0_IN11, CMP_IM_IP4
PA4	17	I/O		Default: PA4 Alternate: TIMER0_CH1, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN10, CMP_IM_IP5
PA7	18	I/O		Default: PA7 Alternate: TIMER19_MCH1, TIMER1_CH1, TIMER19_BRKIN1, TRIGSEL_IN7, EVENTOUT Additional: DAC_OUT
PB1	19	I/O		Default: PB1 Alternate: TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: ADC0_IN9(5)
PE10	20	I/O		Default: PE10 Alternate: TIMER7_BRKIN2, EVENTOUT, I2C1_SCL Additional: ADC0_IN14
PE11	21	I/O		Default: PE11 Alternate: TIMER7_MCH1, TRIGSEL_IN8, EVENTOUT, I2C1_SDA Additional: ADC0_IN13
PE12	22	I/O		Default: PE12 Alternate: TIMER7_CH1, TRIGSEL_IN9, EVENTOUT, I2C1_SMBA Additional: ADC0_IN12
PE13	23	I/O		Default: PE13 Alternate: TIMER7_MCH0, TIMER7_CH0, SPI0_MISO, TRIGSEL_IN2, EVENTOUT Additional: ADC0_IN7
PE14	24	I/O		Default: PE14 Alternate: TIMER7_CH0, TIMER7_CH1, SPI0_SCK, TRIGSEL_IN3, EVENTOUT Additional: ADC0_IN6
PB13	25	I/O		Default: PB13 Alternate: TIMER_ETI0(3), SPI0_MOSI, USART0_TX, CAN0_TX, EVENTOUT Additional: ADC0_IN5, ADC1_IN15(5)
PB14	26	I/O		Default: PB14 Alternate: TIMER1_CH2, SPI0_NSS, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN4, ADC1_IN14(5)

GD32A503Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB15	27	I/O		Default: PB15 Alternate: TIMER7_BRKIN1, USART1_TX, USART0_RTS, USART0_DE, EVENTOUT
PD8	28	I/O		Default: PD8 Alternate: TIMER7_BRKIN0, USART1_RX, USART0_CTS, EVENTOUT
PD9	29	I/O		Default: PD9 Alternate: TIMER0_BRKIN2, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC0_IN3
VSS_2	30	P		Default: VSS_2
VDD_2	31	P		Default: VDD_2
PC7	32	I/O		Default: PC7 Alternate: TIMER0_MCH0, TIMER20_BRKIN1(6), I2S1_MCK, EVENTOUT Additional: ADC1_IN8, ADC0_IN8(5)
PA8	33	I/O		Default: PA8 Alternate: TIMER0_BRKIN0, TIMER20_MCH2(6), SPI1_NSS, I2S1_WS, MFCOM_D7, MFCOM_D5, TRIGSEL_IN4, EVENTOUT Additional: ADC1_IN3, NMI
PA9	34	I/O		Default: PA9 Alternate: TIMER20_CH2(6), SPI1_MOSI, I2S1_SD, MFCOM_D6, MFCOM_D4, TRIGSEL_IN5, EVENTOUT Additional: ADC1_IN2
PA10	35	I/O		Default: PA10 Alternate: TIMER20_MCH0(6), I2C0_SCL, USART0_TX, MFCOM_D5, EVENTOUT Additional: ADC1_IN1
PA11	36	I/O		Default: PA11 Alternate: TIMER20_CH0(6), I2C0_SDA, USART0_RX, MFCOM_D4, EVENTOUT, TRIGSEL_IN13 Additional: ADC1_IN0
PC10	37	I/O		Default: PC10 Alternate: TIMER7_MCH0, TIMER7_CH0, I2C0_SDA, USART0_RTS, USART0_DE, MFCOM_D3, TRIGSEL_OUT0, EVENTOUT Additional: ADC0_IN1, CMP_IM_IP1
PC11	38	I/O		Default: PC11 Alternate: TIMER19_MCH0, TIMER19_CH0, I2C0_SCL, USART0_CTS, MFCOM_D2, TRIGSEL_OUT3,

GD32A503Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT Additional: ADC0_IN0, CMP_IM_IP0
PC12	39	I/O		Default: PC12 Alternate: TIMER20_MCH1(6), TIMER7_CH0, USART1_TX, CAN1_TX, EVENTOUT Additional: ADC1_IN5
PD0	40	I/O		Default: PD0 Alternate: TIMER20_CH1(6), TIMER7_CH1, USART1_RX, CAN1_RX, EVENTOUT Additional: ADC1_IN4
PD6	41	I/O		Default: PD6 Alternate: TIMER7_MCH3, TIMER19_CH0, CAN1_TX, EVENTOUT, I2C1_SCL
PD7	42	I/O		Default: PD7 Alternate: TIMER7_CH3, TIMER19_CH1, CAN1_RX, EVENTOUT, I2C1_SDA
PB3	43	I/O		Default: NJTRST, PB3 Alternate: TIMER7_MCH2, SPI0_IO2, MFCOM_D1, EVENTOUT
PB4	44	I/O		Default: JTDO, PB4 Alternate: TIMER7_CH2, SPI0_IO3, MFCOM_D0, EVENTOUT
PB7	45	I/O		Default: JTDI, PB7 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT, I2C1_SCL
PB8	46	I/O		Default: JTCK, SWCLK, PB8 Alternate: TIMER7_CH0, TIMER7_CH1, EVENTOUT, I2C1_SDA Additional: CMP_IM_IP2
NRST	47	I/O		Default: NRST
PB9	48	I/O		Default: JTMS, SWDIO, PB9 Alternate: CMP_OUT, EVENTOUT, I2C1_SMBA Additional: BOOT1

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) This function is controlled by SYSCFG_TIMERINSEL register.

(4) This function is controlled by SYSCFG_CFG0 register.

(5) This function is controlled by SYSCFG_CFG1 register.

(6) Functions are available on GD32A503CC devices only.

2.6.4. GD32A503Kx QFN32 pin definitions

Table 2-6. GD32A503Kx QFN32 pin definitions

GD32A503Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC15	1	I/O		Default: PC15 Alternate: TIMER_ETI2(3), TIMER19_MCH1, TIMER19_CH1, CAN0_TX, MFCOM_D7, EVENTOUT
PF0-BOOT0	2	I/O		Default: PF0(4) Alternate: TIMER19_CH1, CAN0_RX, MFCOM_D6, EVENTOUT Additional: BOOT0
VDD	3	P		Default: VDD
VSS	4	P		Default: VSS
PF6-OSCOUT	5	I/O		Default: PF6 Alternate: I2C0_SCL, EVENTOUT Additional: OSCOUT
PF7-OSCIN	6	I/O		Default: PF7 Alternate: I2C0_SDA, EVENTOUT Additional: OSCIN
PF5	7	I/O		Default: PF5 Alternate: TIMER0_MCH0, SPI0_MISO, EVENTOUT
PC0	8	I/O		Default: PC0 Alternate: TIMER0_CH0, SPI0_SCK, EVENTOUT
PA0-WKUP	9	I/O		Default: PA0 Alternate: TIMER0_CH3, EVENTOUT Additional: CMP_IM_IP3, WKUP0
PA1	10	I/O		Default: PA1 Alternate: CK_OUT, TIMER0_MCH2, SPI0_NSS, TRIGSEL_IN0, EVENTOUT
PA2	11	I/O		Default: PA2 Alternate: TIMER0_CH2, SPI0_MOSI, TRIGSEL_IN1, EVENTOUT
PA3	12	I/O		Default: PA3 Alternate: TIMER0_MCH1, USART0_TX, CAN0_TX, TIMER1_CH3, EVENTOUT Additional: ADC0_IN11, CMP_IM_IP4
PA4	13	I/O		Default: PA4 Alternate: TIMER0_CH1, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN10, CMP_IM_IP5
PA7	14	I/O		Default: PA7 Alternate: TIMER19_MCH1, TIMER1_CH1,

GD32A503Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER19_BRKIN1, TRIGSEL_IN7, EVENTOUT Additional: DAC_OUT
PE13	15	I/O		Default: PE13 Alternate: TIMER7_MCH0, TIMER7_CH0, SPI0_MISO, TRIGSEL_IN2, EVENTOUT Additional: ADC0_IN7
PE14	16	I/O		Default: PE14 Alternate: TIMER7_CH0, TIMER7_CH1, SPI0_SCK, TRIGSEL_IN3, EVENTOUT Additional: ADC0_IN6
PB13	17	I/O		Default: PB13 Alternate: TIMER_ETI0(3), SPI0_MOSI, USART0_TX, CAN0_TX, EVENTOUT Additional: ADC0_IN5, ADC1_IN15(5)
PB14	18	I/O		Default: PB14 Alternate: TIMER1_CH2, SPI0_NSS, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN4, ADC1_IN14(5)
PD9	19	I/O		Default: PD9 Alternate: TIMER0_BRKIN2, EVENTOUT Additional: ADC0_IN3
VSS_2	20	P		Default: VSS_2
VDD_2	21	P		Default: VDD_2
PA8	22	I/O		Default: PA8 Alternate: TIMER0_BRKIN0, TIMER20_MCH2(6), MFCOM_D7, MFCOM_D5, TRIGSEL_IN4, EVENTOUT Additional: ADC1_IN3, NMI
PA10	23	I/O		Default: PA10 Alternate: TIMER20_MCH0(6), I2C0_SCL, USART0_TX, MFCOM_D5, EVENTOUT Additional: ADC1_IN1
PA11	24	I/O		Default: PA11 Alternate: TIMER20_CH0(6), I2C0_SDA, USART0_RX, MFCOM_D4, EVENTOUT, TRIGSEL_IN13 Additional: ADC1_IN0
PC10	25	I/O		Default: PC10 Alternate: TIMER7_MCH0, TIMER7_CH0, I2C0_SDA, USART0_RTS, USART0_DE, MFCOM_D3, TRIGSEL_OUT0, EVENTOUT Additional: ADC0_IN1, CMP_IM_IP1
PC11	26	I/O		Default: PC11 Alternate: TIMER19_MCH0, TIMER19_CH0, I2C0_SCL,

GD32A503Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				USART0_CTS, MFCOM_D2, TRIGSEL_OUT3, EVENTOUT Additional: ADC0_IN0, CMP_IM_IP0
PB3	27	I/O		Default: NJTRST, PB3 Alternate: TIMER7_MCH2, SPI0_IO2, MFCOM_D1, EVENTOUT
PB4	28	I/O		Default: JTDO, PB4 Alternate: TIMER7_CH2, SPI0_IO3, MFCOM_D0, EVENTOUT
PB7	29	I/O		Default: JTDI, PB7 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT, I2C1_SCL
PB8	30	I/O		Default: JTCK, SWCLK, PB8 Alternate: TIMER7_CH0, TIMER7_CH1, EVENTOUT, I2C1_SDA Additional: CMP_IM_IP2
NRST	31	I/O		Default: NRST
PB9	32	I/O		Default: JTMS, SWDIO, PB9 Alternate: CMP_OUT, EVENTOUT, I2C1_SMBA Additional: BOOT1

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) This function is controlled by SYSCFG_TIMERINSEL register.

(4) This function is controlled by SYSCFG_CFG0 register.

(5) This function is controlled by SYSCFG_CFG1 register.

(6) Functions are available on GD32A503KC devices only.

2.6.5. GD32A503xx pin alternate functions

Table 2-7. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PA0		TIMER0_CH3								EVENTOUT
PA1	CK_OUT	TIMER0_MCH2			SPI0_NSS			TRIGSEL_IN0		EVENTOUT
PA2		TIMER0_CH2			SPI0_MOSI			TRIGSEL_IN1		EVENTOUT
PA3		TIMER0_MCH1	TIMER1_CH3			USART0_TX	CAN0_TX			EVENTOUT
PA4		TIMER0_CH1				USART0_RX	CAN0_RX			EVENTOUT
PA5			TIMER19_BRKIN3			USART2_TX				EVENTOUT
PA6			TIMER19_BRKIN2			USART2_RX				EVENTOUT
PA7		TIMER19_MCH1	TIMER1_CH1	TIMER19_BRKIN1		USART2_CK(3)		TRIGSEL_IN7		EVENTOUT
PA8		TIMER0_BRKIN0	TIMER20_MCH2(4)		SPI1_NSS(2)/I2S1_WS(2)	MFCOM_D7	MFCOM_D5	TRIGSEL_IN4		EVENTOUT
PA9		TIMER20_CH2(4)			SPI1_MOSI/I2S1_SD	MFCOM_D6	MFCOM_D4	TRIGSEL_IN5		EVENTOUT
PA10		TIMER20_MCH0(4)		I2C0_SCL		USART0_TX	MFCOM_D5			EVENTOUT
PA11		TIMER20_CH0(4)		I2C0_SDA		USART0_RX	MFCOM_D4	TRIGSEL_IN13		EVENTOUT
PA12		TIMER20_MCH1		I2C0_SMBA		USART0_CK				EVENTOUT
PA13		TIMER20_CH1		I2C0_SDA						EVENTOUT
PA14		TIMER20_MCH0		I2C0_SCL						EVENTOUT
PA15		TIMER20_CH0						TRIGSEL_IN12		EVENTOUT

Table 2-8. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PB0		TIMER19_	TIMER19_							EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
		CH0	CH1							
PB1		TIMER0_MCH0	TIMER7_MCH3							EVENTOUT
PB2		TIMER0_CH0	TIMER7_CH3							EVENTOUT
PB3	NJTRST	TIMER7_MCH2			SPI0_IO2		MFCOM_D1			EVENTOUT
PB4	JTDO	TIMER7_CH2			SPI0_IO3		MFCOM_D0			EVENTOUT
PB5			TIMER7_BRKIN1	I2C0_SMBA	SPI0_MISO	SPI1_NSS/I2S1_WS				EVENTOUT
PB6			TIMER7_BRKIN2	TIMER_ETI1(1)	SPI0_SCK	SPI1_MOSI/I2S1_SD				EVENTOUT
PB7	JTDI	TIMER19_CH0	TIMER19_CH1			I2C1_SCL				EVENTOUT
PB8	JTCK/SWCLK	TIMER7_CH0	TIMER7_CH1			I2C1_SDA				EVENTOUT
PB9	JTMS/SWDIO					I2C1_SMBA		CMP_OUT		EVENTOUT
PB10		TIMER20_CH3	TIMER19_CH3		SPI0_IO3	USART2_CTS				EVENTOUT
PB11		TIMER20_MCH2	TIMER1_CH3					TRIGSEL_IN10		EVENTOUT
PB12		TIMER20_CH2						TRIGSEL_IN11		EVENTOUT
PB13	TIMER_ETI0(1)				SPI0_MOSI	USART0_TX	CAN0_TX			EVENTOUT
PB14		TIMER1_CH2			SPI0_NSS	USART0_RX	CAN0_RX			EVENTOUT
PB15			TIMER7_BRKIN1		USART1_TX	USART0_RTS/USART0_DE				EVENTOUT

Table 2-9. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PC0		TIMER0_CH0			SPI0_SCK					EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PC1		TIMER0_MCH3				USART2_CTS(3)				EVENTOUT
PC2	CK_OUT	TIMER19_MCH2				USART1_TX				EVENTOUT
PC3		TIMER19_CH2				USART1_RX				EVENTOUT
PC4		TIMER19_CH1				USART2_RTS/ USART2_DE				EVENTOUT
PC5		TIMER19_MCH0	TIMER19_CH0			USART2_CTS				EVENTOUT
PC6		TIMER0_CH1			SPI1_SCK/ I2S1_CK					EVENTOUT
PC7		TIMER0_MCH0	TIMER20_BRKIN1(4)		I2S1_MCK					EVENTOUT
PC8		TIMER0_CH0	TIMER20_BRKIN2(4)							EVENTOUT
PC9		TIMER0_BRKIN3	TIMER20_BRKIN3(4)							EVENTOUT
PC10		TIMER7_MCH0	TIMER7_CH0	I2C0_SDA		USART0_RTS/ USART0_DE	MFCOM_D3	TRIGSEL_OUT0		EVENTOUT
PC11		TIMER19_MCH0	TIMER19_CH0	I2C0_SCL		USART0_CTS	MFCOM_D2	TRIGSEL_OUT3		EVENTOUT
PC12		TIMER20_MCH1(4)	TIMER7_CH0			USART1_TX	CAN1_TX			EVENTOUT
PC13	CK_OUT		TIMER19_CH2				MFCOM_D4	TRIGSEL_OUT4		EVENTOUT
PC14			TIMER19_BRKIN0							EVENTOUT
PC15	TIMER_ETI2(1)	TIMER19_MCH1	TIMER19_CH1				CAN0_TX	MFCOM_D7		EVENTOUT

Table 2-10. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PD0		TIMER20_CH1(4)	TIMER7_CH1			USART1_RX	CAN1_RX			EVENTOUT
PD1		TIMER7_M			SPI1_NSS/					EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
		CH1			I2S1_WS					
PD2		TIMER7_CH1			SPI0_NSS					EVENTOUT
PD3		TIMER20_MCH3(4)			SPI0_NSS	USART1_RTS/ USART1_DE				EVENTOUT
PD4		TIMER20_CH3(4)	TIMER1_CH2		SPI0_MOSI	USART1_CTS				EVENTOUT
PD5		TIMER0_BRKIN0	TIMER20_BRKIN1	TIMER7_BRKIN0		USART1_CK				EVENTOUT
PD6		TIMER7_MCH3	TIMER19_CH0			I2C1_SCL	CAN1_TX			EVENTOUT
PD7		TIMER7_CH3	TIMER19_CH1			I2C1_SDA	CAN1_RX			EVENTOUT
PD8			TIMER7_BRKIN0		USART1_RX	USART0_CTS				EVENTOUT
PD9			TIMER0_BRKIN2			USART1_RTS(2) / USART1_DE(2)				EVENTOUT
PD10			TIMER0_BRKIN1		SPI1_NSS/ I2S1_WS	USART1_CTS				EVENTOUT
PD11		TIMER0_MCH3	TIMER20_BRKIN0(4)			I2C1_SMBA				EVENTOUT
PD12		TIMER0_CH3	TIMER20_BRKIN0							EVENTOUT
PD13		TIMER0_MCH2			SPI1_NSS/ I2S1_WS					EVENTOUT
PD14		TIMER0_CH2			SPI1_MOSI/I2S1_SD					EVENTOUT
PD15		TIMER0_MCH1			SPI1_MISO					EVENTOUT

Table 2-11. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PE0		TIMER20_BRKIN2	TIMER7_BRKIN3			USART2_TX	MFCOM_D7			EVENTOUT
PE1		TIMER20_BRKIN3				USART2_RX	MFCOM_D6			EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PE2			TIMER19_MCH3			USART1_RTS/ USART1_DE	MFCOM_D3	TRIGSEL_OUT7		EVENTOUT
PE3			TIMER19_CH3			USART1_CTS	MFCOM_D2	TRIGSEL_OUT6		EVENTOUT
PE4		TIMER0_MCH1	TIMER19_MCH0		SPI1_MISO		MFCOM_D1	TRIGSEL_OUT2		EVENTOUT
PE5		TIMER0_CH1	TIMER19_CH0		SPI1_SCK/ I2S1_CK		MFCOM_D0	TRIGSEL_OUT1		EVENTOUT
PE6		TIMER1_CH0, TIMER1_ETI	TIMER19_MCH2		I2S1_MCK		MFCOM_D5	TRIGSEL_OUT5		EVENTOUT
PE7		TIMER7_MCH2	TIMER19_BRKIN3				MFCOM_D0			EVENTOUT
PE8		TIMER7_CH2	TIMER19_BRKIN2				MFCOM_D1			EVENTOUT
PE9			TIMER7_BRKIN3							EVENTOUT
PE10			TIMER7_BRKIN2			I2C1_SCL				EVENTOUT
PE11		TIMER7_MCH1				I2C1_SDA		TRIGSEL_IN8		EVENTOUT
PE12		TIMER7_CH1				I2C1_SMBA		TRIGSEL_IN9		EVENTOUT
PE13		TIMER7_MCH0	TIMER7_CH0		SPI0_MISO			TRIGSEL_IN2		EVENTOUT
PE14		TIMER7_CH0	TIMER7_CH1		SPI0_SCK			TRIGSEL_IN3		EVENTOUT
PE15		TIMER20_MCH3	TIMER19_MCH3		SPI0_IO2	USART2_RTS/ USART2_DE				EVENTOUT

Table 2-12. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PF0		TIMER19_CH1					CAN0_RX	MFCOM_D6		EVENTOUT
PF1		TIMER0_B	TIMER19_							EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
		RKIN1	BRKIN1							
PF2		TIMER0_BRKIN0	TIMRE19_BRKIN0			USART2_RTS/ USART2_DE	TRIGSEL_IN6	CMP_OUT		EVENTOUT
PF3			TIMER0_BRKIN3			USART2_TX				EVENTOUT
PF4			TIMER0_BRKIN2			USART2_RX				EVENTOUT
PF5		TIMER0_MCH0			SPI0_MISO	USART1_CTS(2)				EVENTOUT
PF6				I2C0_SCL						EVENTOUT
PF7				I2C0_SDA						EVENTOUT

Notes:

(1) This function is controlled by SYSCFG_TIMERINSEL register.

(2) Functions are available on GD32A503Vx/Rx/Cx devices only.

(3) Functions are available on GD32A503Vx/Rx devices only.

(4) Functions are available on GD32A503xC/xD/VB devices only.

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption.

32-bit Arm® Cortex®-M33 processor core

- Up to 100 MHz operation frequency
- Ultra-low power, energy-efficient operation
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M33 processor is based on the ARMv8 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit (BPU)
- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Memory Protection Unit (MPU)
- Floating Point Unit (FPU)
- DSP Extension (DSP)

3.2. Embedded memory

- Up to 384 Kbytes of Flash memory
- Max 4KB emulated EEPROM
- Extend Block: 64KB shared for data flash and EEPROM backup
- 4KB shared RAM for basic SRAM or EEPROM SRAM or fast program buffer
- ECC of on-chip Flash memory with single bit error corrected and double bit errors detected
- Up to 48 Kbytes of SRAM with ECC check

384 Kbytes of inner Flash and 48 Kbytes of inner SRAM at most is available for storing programs and data. 0~3 waiting time within Bank0/Bank1/Data Flash when CPU executes

instructions and data. ***Table 2-2. GD32A503xx memory map*** shows the memory map of the GD32A503xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 2 to 40 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.7 to 5.5 V application supply and I/Os

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 100 MHz/100 MHz/50 MHz. See ***Figure 2-6. GD32A503xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCTL) controls three kinds of reset: system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller and the backup domain. Power-on reset (POR) and power-down reset (PDR) are always active. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security. The embedded over voltage detector (OVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.7 to 5.5 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} range: 2.7 to 5.5 V, external analog power supplies for ADC, DAC, reset blocks, RCs and PLL.
- V_{BAK} range: 2.7 to 5.5 V, power supply for RTC, external clock 32 kHz oscillator, backup registers and three pads, including PC13 to PC15.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory

by using USART0 (PA10 and PA11), LIN (PA3 and PA4), and CAN0 (PB13 and PB14).

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep, Deep-sleep, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.1V domain are off, and all of IRC8M, HXTAL and PLLs are disabled. The contents of SRAM and registers are preserved. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, LVD output, CAN0 wakeup, CAN1 wakeup, USART0 wakeup, USART1 wakeup, USART2 wakeup, CMP output and over voltage output. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.1V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pins.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: VREFP to VREFN
- Temperature sensor

Two 12-bit 1 MSPS multi-channel ADCs are integrated in the device. It has a total of 18 multiplexed channels: up to 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}) and 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between VREFP and VREFN. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered by TRIGSEL, or by software. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC and DAC, the ADC/DAC independent external reference voltage should be connected to VREFP/VREFN pins. According to the different packages, VREFP pin can be connected to V_{DDA} pin, or external reference voltage, VREFN pin must be connected to V_{SS} pin. The VREFP pin is only available on no less than 64-pin packages, or else the VREFP pin is not available and internally connected to V_{DDA}. The VREFN pin is only available on no less than 100-pin packages, or else the VREFN pin is not available and internally connected to V_{SS}.

3.7. Digital to analog converter (DAC)

- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC is used to generate variable analog outputs. The DAC channel can be triggered by TRIGSEL or by software with DMA support. The maximum output value of the DAC is VREFP.

3.8. Controller area network (CAN)

- Two CAN interfaces supports the CAN protocols version 2.0A and B, ISO11891-1:2015 and BOSCH CAN FD specification with baud rates up to 1 Mbit/s when classical frames and 8 Mbit/s when FD frames.
- Supports CAN FD Frame with up to 64 data bytes (ISO11898-1 and Bosch CAN FD specification V1.0).
- Supports four communication mode: normal mode, Inactive mode, Loopback and silent mode, and Monitor mode.
- 32 mailboxes when configures with 8 bytes data length each, configurable as Rx or Tx mailbox.
- Receive public filter register for Rx mailboxes and receive public filter register for Rx FIFO.

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. The CAN module is a CAN Protocol controller with a very flexible mailbox system for transmitting and receiving CAN frames. The mailbox system consists of a set of mailboxes that store configuration and control data, timestamp, message ID, and data. The space of up to 32 mailboxes can also be configured as Rx FIFO with ID filtering against up to 104 extended IDs or 208 standard IDs or 416 partial 8-bit IDs, and configure receive FIFO/mailbox private filter register for up to 32 ID filter table elements.

3.9. Comparators (CMP)

- One fast rail-to-rail low-power comparator with software configurable
- Comparator has configurable analog input source

One Comparator (CMP) is implemented within the devices. It can work either standalone (all terminal are available on I/Os) or together with the timers. It could be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieves some current control by working together with a PWM output of a timer and the DAC. It blanking function can be used for false overcurrent detection in motor control applications.

3.10. Direct memory access controller (DMA)

- 7 channels for DMA0 controller and 5 channels for DMA1 controller, and each channel are configurable
- Each channel is connected to flexible hardware DMA request.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to flexible hardware DMA requests. Each channel is dedicated to manage memory access requests from one or more peripherals. Transfer size of source and destination are independent and configurable.

3.11. DMA request multiplexer (DMAMUX)

- 12 channels for DMAMUX request multiplexer and 4 channels for DMAMUX request generator
- Support 27 trigger inputs
- Support 27 synchronization inputs

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

3.12. General-purpose inputs/outputs (GPIOs)

- Up to 88 fast GPIOs, all mappable on 16 external interrupt lines

- Analog input/output configurable
- Alternate function input/output configurable

There are up to 88 general purpose I/O pins (GPIO) in GD32A503xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, and PF0 ~ PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.13. Inter-integrated circuit (I2C)

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 3.0 and PMBus 1.3 compatible

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.14. Inter-IC sound (I2S)

- One I2S bus Interface with sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32A503xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.15. Multi-function communication Interface (MFCOM)

- Programmable logic mode by integrating external digital logic function chip or combining

pin / shifter / timer function to produce complex output.

- USART, I2C, SPI, I2S, PWM waveform generation supported

The MFCOM is a highly configurable module provide emulation of a variety of serial communication protocols and flexible timers. Data can be signaled by timer, loaded, stored and compared between shifter and shiftbuf using DMA/Polling/Interrupt method. Program trigger, pin or shifter flag for the timer to produce shift clock that transfers data and generate specific events.

3.16. Real time clock (RTC)

- 32-bit programmable counter with a programmable 20-bit prescaler
- Alarm function

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock of HXTAL clock divided by 128, or LXTAL oscillator clock, or IRC40K oscillator clock.

3.17. Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 22.5 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad-SPI configuration available in master mode (only in SPI0)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

3.18. Trigger selection controller (TRIGSEL)

- Trigger input source could be external input signal or output of peripheral
- Trigger selection output could be for external output or peripheral
- Supports different optional trigger inputs

The trigger selection controller (TRIGSEL) allows software to select the trigger input signal for various peripherals. TRIGSEL provides a flexible mechanism for a peripheral to select different trigger inputs. With TRIGSEL, there are up to 4 trigger selection outputs could be selected for each peripheral. And every output could select from different trigger input signal.

3.19. Timers and PWM generation

- Four 16-bit advanced timer (TIMER0, TIMER7, TIMER19, TIMER20), one 16-bit general timer (TIMER1), and two 16-bit basic timer (TIMER5, TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0, TIMER7, TIMER19, TIMER20) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 8 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMER1. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 &TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32A503xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep, and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.20. Universal synchronous asynchronous receiver transmitter (USART)

- Maximum speed up to 12.5 MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.21. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.22. Package and operation temperature

- LQFP100(GD32A503Vx), LQFP64 (GD32A503Rx), LQFP48(GD32A503Cx) and QFN32(GD32A503Kx).
- Operation temperature range: -40°C to +125°C (automotive level).

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1) (4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 5.5	V
V_{IN}	Input voltage on all I/O pins(3)	V_{SS} - 0.3	V_{DD} + 0.3	V
$\|\Delta V_{DDX}\|$	Variations between different VDD power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±35	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	110	
I_{DD}	Maximum current into each VDD pin	—	65	
I_{SS}	Maximum current into each VSS pin	—	65	
$\sum I_{DD}$	Total current into all VDD pins	—	160	
$\sum I_{SS}$	Total current into all VSS pins	—	160	
T_A	Operating temperature range	-40	+125	°C
P_D	Power dissipation at T_A = 125°C of LQFP100	—	441	mW
	Power dissipation at T_A = 125°C of LQFP64	—	482	
	Power dissipation at T_A = 125°C of LQFP48	—	483	
	Power dissipation at T_A = 125°C of QFN32	—	674	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	150	°C

(1) Guaranteed by design, not tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) V_{IN} maximum value cannot exceed 5.5 V.
(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

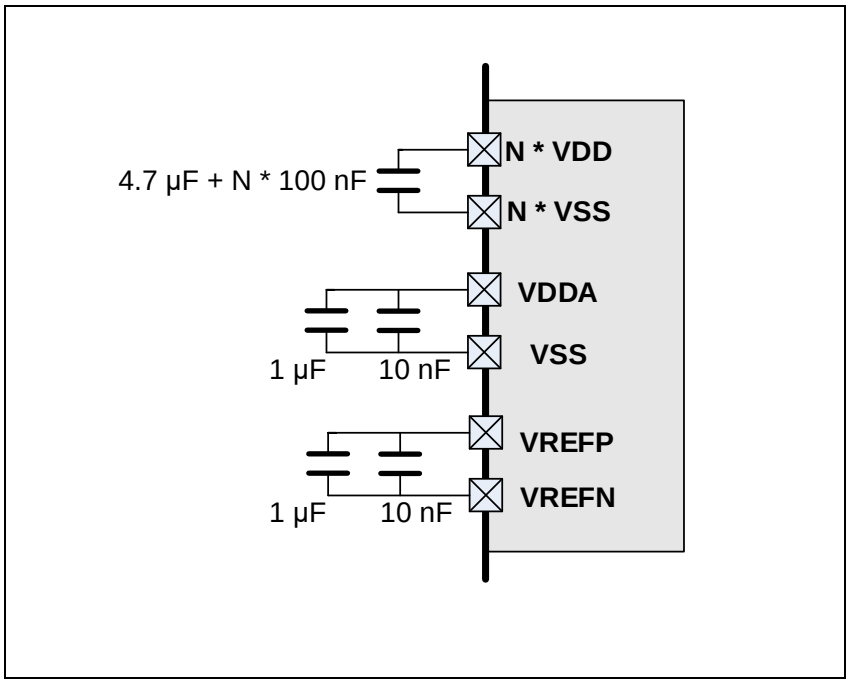
4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}(2)	Supply voltage	—	2.7	5.0	5.5	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.7	5.0	5.5	V

(1) Guaranteed by design, not tested in production.
(2) If the voltage is below 3V, the flash erasing may be interrupted and FMC_STAT0->RSTERR=1.

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)



(1) The VREFP and VREFN pins are only available on 100-pin package, or else the VREFP/ VREFN pins are not available and internally connected to VDDA and VSS pins. More details refer to ***AN110 GD32A503 Hardware Development Guide***.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	—	—	100	MHz
f_{APB1}	APB1 clock frequency	—	—	50	MHz
f_{APB2}	APB2 clock frequency	—	—	100	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up / Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs/V
	V_{DD} fall time rate		100	∞	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL (HXTALSCAL off)	5.2	ms
		Clock source from HXTAL (HXTALSCAL on)	2.1	ms
		Clock source from IRC8M	105	us

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics(1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	1.3	μs
$t_{Deep-sleep}$(3)	Wakeup from Deep-sleep mode（LDO in normal power mode and normal driver mode）	2.3	
	Wakeup from Deep-sleep mode（LDO in low power mode and normal driver mode）	2.3	
	Wakeup from Deep-sleep mode（LDO in normal power mode and low driver mode）	2.3	
	Wakeup from Deep-sleep mode（LDO in low power mode and low driver mode）	2.3	
$t_{Standby}$	Wakeup from Standby mode	110	

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 5 V, IRC8M = System clock = 8 MHz.

(3) DSLPVS[1:0] bit in Register RCU_DSV is 0x11.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics (2)(3)(4)(5)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 100 MHz, All peripherals enabled	—	24.6	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 100 MHz, All peripherals disabled	—	11.9	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals enabled	—	18.5	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals disabled	—	9.3	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 64 MHz, All peripherals enabled	—	15	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 64 MHz, All peripherals disabled	—	6.7	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled	—	11.6	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled	—	5.4	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 32 MHz, All peripherals enabled	—	8.3	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 32 MHz, All peripherals disabled	—	4.2	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled	—	6.7	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled	—	3.5	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled	—	5	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled	—	2.9	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled	—	3.3	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals disabled	—	2.2	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 4 MHz, All peripherals enabled	—	2.5	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 4 MHz, All peripherals disabled	—	1.9	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock =2 MHz, All peripherals enabled	—	2	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 2 MHz, All peripherals disabled	—	1.7	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 1 MHz, All peripherals enabled	—	1.8	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 1 MHz, All peripherals disabled	—	1.6	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 100 MHz, CPU clock off, All peripherals enabled	—	19.7	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 100 MHz, CPU clock off, All peripherals disabled	—	6.1	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 72 MHz, CPU clock off, All peripherals enabled	—	14.7	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 72 MHz, CPU clock off, All peripherals disabled	—	4.8	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 64 MHz, CPU clock off, All peripherals enabled	—	13.3	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 64 MHz, CPU clock off, All peripherals disabled	—	4.5	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 48 MHz, CPU clock off, All peripherals enabled	—	10.3	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 48 MHz, CPU clock off, All peripherals disabled	—	3.7	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 32 MHz, CPU clock off, All peripherals enabled	—	7.5	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 32 MHz, CPU clock off, All peripherals disabled	—	3	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 24 MHz, CPU clock off, All peripherals enabled	—	6	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 24 MHz, CPU clock off, All peripherals disabled	—	2.7	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 16 MHz, CPU clock off, All peripherals enabled	—	4.6	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 16 MHz, CPU clock off, All peripherals disabled	—	2.3	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 8 MHz, CPU clock off, All peripherals enabled	—	3.1	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 8 MHz, CPU clock off, All peripherals disabled	—	2	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 4 MHz, CPU clock off, All peripherals enabled	—	2.4	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 4 MHz, CPU clock off, All peripherals disabled	—	1.7	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 2 MHz, CPU clock off, All peripherals enabled	—	2	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 2 MHz, CPU clock off, All peripherals disabled	—	1.6	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 1 MHz, CPU clock off, All peripherals enabled	—	1.8	—	mA
		V_{DD} = V_{DDA} = 5 V, HXTAL = 8 MHz, System clock = 1 MHz, CPU clock off, All peripherals disabled	—	1.58	—	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 5 V, LDO in normal power and normal driver mode, FMC_WS_SLEEP_SLP = 1, IRC40K off, RTC off, SRAM1 and SRAM2 on, V_{core} = 1.1V	—	182.50	—	uA
		V_{DD} = V_{DDA} = 5 V, LDO in low power and normal driver mode, FMC_WS_SLEEP_SLP = 1, RTC off, SRAM1 and SRAM2 on, V_{core} = 1.1V	—	130.60	—	uA
		V_{DD} = V_{DDA} = 5 V, LDO in normal power and low driver mode, FMC_WS_SLEEP_SLP = 1, IRC40K off, RTC off, SRAM1 and SRAM2 on, V_{core} = 1.1V	—	103.93	—	uA
		V_{DD} = V_{DDA} = 5 V, LDO in low power and low driver mode, FMC_WS_SLEEP_SLP = 1, IRC40K off, RTC off, SRAM1 and SRAM2 on, V_{core} = 1.1V	—	76.77	—	uA
		V_{DD} = V_{DDA} = 5 V, LDO in low power and low driver mode, FMC_WS_SLEEP_SLP = 1, IRC40K off, RTC off, SRAM1 and SRAM2 off, V_{core} = 0.8V	—	41.63	—	uA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 5 V, IRC40K on, RTC on, BOR on	—	8.59	—	μA
		V_{DD} = V_{DDA} = 5 V, IRC40K on, RTC off, BOR on	—	7.65	—	μA
		V_{DD} = V_{DDA} = 5 V, IRC40K off, RTC off, BOR on	—	6.11	—	μA
		V_{DD} = V_{DDA} = 5 V, IRC40K off, RTC off, BOR off	—	2.31	—	μA

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for T_A = 25 °C and test result is mean value.

(3) Run mode and sleep mode use WS_WSCNT_3 and PLL on.

(4) When analog peripheral blocks such as ADCs, DACs, HXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

(5) All GPIOs are configured as analog mode except standby mode.

Figure 4-2. Typical supply current consumption in Run mode

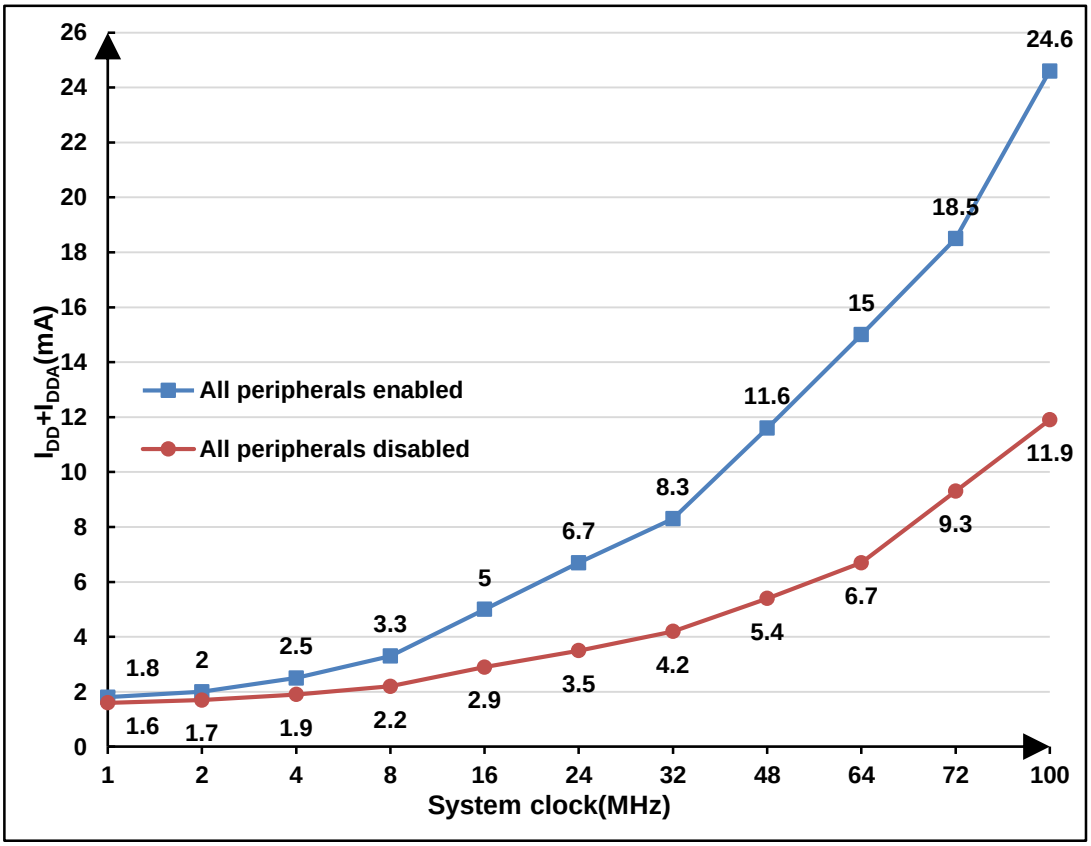
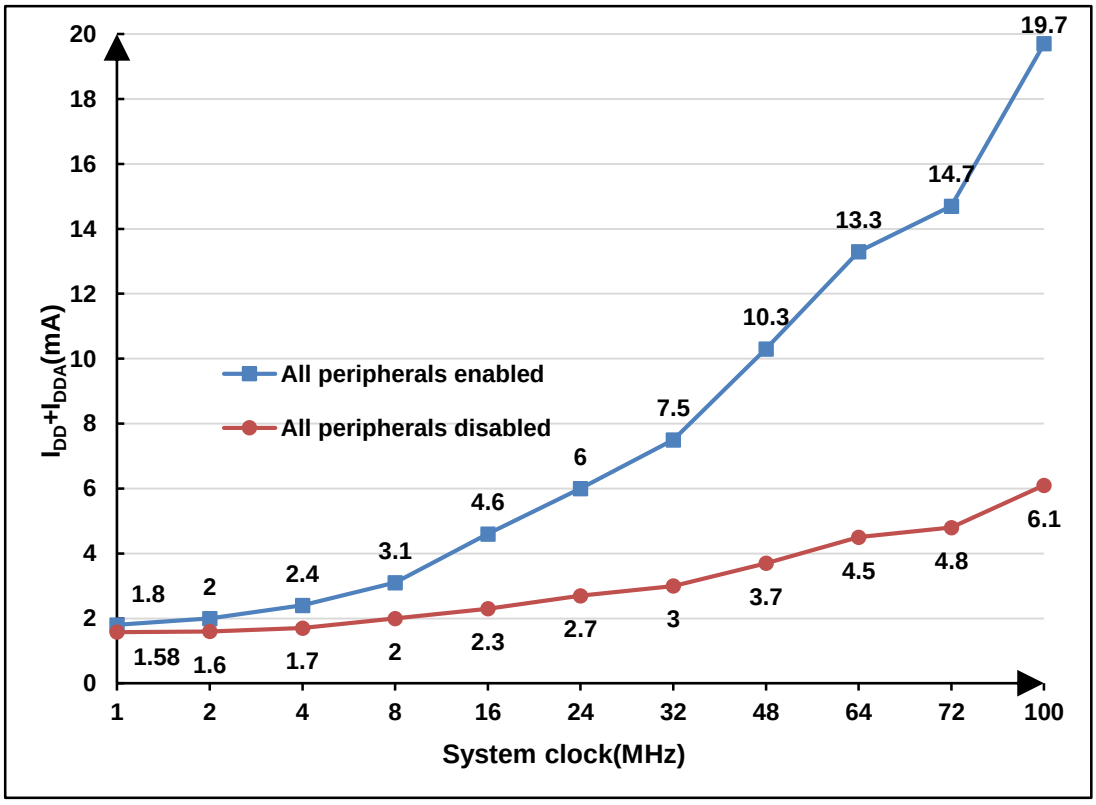


Figure 4-3. Typical supply current consumption in Sleep mode



4.4. EMC characteristics

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-8. EMI characteristics***, The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-8. EMI characteristics(1)

Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}] 8/100 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 5.5 V, T_A = +25 °C, LQFP100, f_{HCLK} = 100 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-8.64	dBµV
			30 MHz to 130 MHz	12.84	
			130 MHz to 1 GHz	30.60	
			1 GHz to 3 GHz	11.18	
		V_{DD} = 5.5 V, T_A = +25 °C, LQFP64, f_{HCLK} = 100 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-8.75	
			30 MHz to 130 MHz	12.88	
			130 MHz to 1 GHz	15.91	
			1 GHz to 3 GHz	4.9	
		V_{DD} = 5.5 V, T_A = +21 °C, LQFP48, f_{HCLK} = 100 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-8.66	
			30 MHz to 130 MHz	9.04	
			130 MHz to 1 GHz	10.08	
			1 GHz to 3 GHz	5.85	
		V_{DD} = 5.5 V, T_A = +21 °C, QFN32, f_{HCLK} = 100 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-8.20	
			30 MHz to 130 MHz	2.69	
			130 MHz to 1 GHz	4.87	
			1 GHz to 3 GHz	8.74	

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-9. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	—	2.94	—	V
		LVDT<2:0> = 000(falling edge)	—	2.84	—	
		LVDT<2:0> = 001(rising edge)	—	3.16	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		LVDT<2:0> = 001(falling edge)	—	3.03	—	
		LVDT<2:0> = 010(rising edge)	—	3.36	—	
		LVDT<2:0> = 010(falling edge)	—	3.24	—	
		LVDT<2:0> = 011(rising edge)	—	3.56	—	
		LVDT<2:0> = 011(falling edge)	—	3.44	—	
		LVDT<2:0> = 100(rising edge)	—	4.07	—	
		LVDT<2:0> = 100(falling edge)	—	3.95	—	
		LVDT<2:0> = 101(rising edge)	—	4.27	—	
		LVDT<2:0> = 101(falling edge)	—	4.15	—	
		LVDT<2:0> = 110(rising edge)	—	4.47	—	
		LVDT<2:0> = 110(falling edge)	—	4.35	—	
		LVDT<2:0> = 111(rising edge)	—	4.68	—	
		LVDT<2:0> = 111(falling edge)	—	4.56	—	
$V_{LVDhyst}$(2)	LVD hystersis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	2.13	—	V
V_{PDR}(1)	Power down reset threshold	—	—	2.08	—	V
$V_{PDRhyst}$(1)	PDR hysteresis	—	—	50	—	mV
$t_{RSTTEMPO}$(1)	Reset temporization	—	—	460	—	us
V_{OVD}(1)	OVD threshold (OVDT=1)	Falling edge	—	5.697	—	V
		Rising edge	—	5.714	—	V
$V_{OVDhyst}$(1)	OVD hysteresis (OVDT=1)	—	—	17	—	mV
			—		—	
V_{OVD}(1)	OVD threshold (OVDT=0)	Falling edge	—	5.170	—	V
		Rising edge	—	5.188	—	V
$V_{OVDhyst}$(1)	OVD hysteresis (OVDT=0)	—	—	18	—	mV
V_{BOR}(1)(3)	Brownout threshold	Falling edge	—	2.53	—	V
		Rising edge	—	2.569	—	V
$V_{BORhyst}$(1)	BOR hysteresis	—	—	39	—	mV

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) BOR is not available when V_{DD} is lower than 3V.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-10. ESD and static latch-up characteristics(1) (2) (3)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{ESD(HBM)}$ (4)	Electrostatic discharge voltage (human body model)	T_A = 25 °C, LQFP100, Zap 3 pulse, Zap Interval = 500 ms		—	—	4000	V
$V_{ESD(CDM)}$ (5)	Electrostatic discharge voltage (charge device model)	All pins except the corner pins	T_A = 25 °C, LQFP100	—	—	500	V
		Corner pins only		—	—	750	V
LU (6)	I-test	T_A = 125 °C, LQFP100		—	—	200	mA
	V_{supply} over voltage			—	—	8.25	V

(1) All ESD testing are in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

(2) Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which include the complete DC parametric and functional testing at room temperature and hot temperature”.

(3) Based on characterization, not tested in production.

(4) This parameter is tested in conformity with AEC-Q100-002E.

(5) This parameter is tested in conformity with AEC-Q100-011D.

(6) This parameter is tested in conformity with AEC-Q100-004D.

4.7. External clock characteristics

Table 4-11. High speed external clock (HXTAL) generated from a crystal / ceramic

characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	2.7 V ≤ V_{DD} ≤ 5.5 V	2	8	40	MHz
R_F(2)	Feedback resistor	V_{DD} = 5 V	—	400	—	kΩ
C_{HXTAL}(2) (3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup，RCU_CTL_HXTALSCAL=0	—	4	—	mA/V
		Startup，RCU_CTL_HXTALSCAL=1	—	29	—	
$I_{DDHXTAL}$(1)	Crystal or ceramic operating current	V_{DD} = 5 V, HXTAL SCAL off	—	0.46	—	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 5 V, HXTAL SCAL off	—	5.1	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, for C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-12. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	2.7 V ≤ V_{DD} ≤ 5.5 V	1	—	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 5 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$ (2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$ (2)	OSCIN rise or fall time	—	—	—	10	ns
C_{IN}(2)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ (2)	Duty cycle	—	30	—	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-13. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{LXTAL_ext}(1)	External clock source or oscillator frequency	2.7 V ≤ V_{DD} ≤ 5.5 V	—	—	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	V_{DD} = 5 V	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level		V_{SS}	—	0.3 V_{DD}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	voltage					
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	—	—	—	50	ns
C_{IN}(2)	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$ (2)	Duty cycle	—	30	—	70	%

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-14. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 5 V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 5 V, T_A = -40 °C ~ +125 °C	-3.75	—	+3.75	%
		V_{DD} = V_{DDA} = 5 V, T_A = 25 °C	-1.0	—	+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step(2)	—	—	0.5	—	%
$Ducy_{IRC8M}$(2)	IRC8M oscillator duty cycle		45	50	55	%
$I_{DDAIRC8M}$(1)	IRC8M oscillator operating current		—	107	—	uA
$t_{SUIRC8M}$(1)	IRC8M oscillator startup time		—	1.3	—	us

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-15. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{IRC40K}	Low Speed Internal oscillator (IRC40K) frequency	V_{DD} = V_{DDA} = 5 V, T_A = -40 °C ~ +125 °C	38	—	44	kHz
		V_{DD} = V_{DDA} = 5 V, T_A = 25 °C	38	—	44	
$I_{DDAIRC40K}$	IRC40K oscillator operating current	V_{DD} = V_{DDA} = 5 V	—	0.8	—	μA
$t_{SUIRC40K}$	IRC40K oscillator startup time	V_{DD} = V_{DDA} = 5 V	—	19	—	μs

(1) Based on characterization, not tested in production.

4.9. PLL characteristics

Table 4-16. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	2	—	16	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	100	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	32	—	200	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)(3)	Current consumption on V_{DD}	VCO freq = 200 MHz	—	1100	—	μA
	Current consumption on V_{DDA}		—	620	—	
$Jitter_{PLL}$(4)	Cycle to cycle Jitter(rms)	System clock	—	40	—	ps
	Cycle to cycle Jitter （peak to peak）		—	400	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) PLL clock source = IRC8M/2 = 4 MHz, f_{PLLOUT} = 100 MHz.
(4) Value given with main PLL running.

4.10. Memory characteristics

Table 4-17. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(2)	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	—	100	—	—	kcycles
t_{RET}	Data retention time	—	20	—	—	years
t_{PROG}	Double-Word programming time	T_A = -40°C ~ +125 °C	—	45	—	μs
t_{ERASE}	Sector erase time	T_A = -40°C ~ +125 °C	1	—	20	ms
$t_{MERASE(256K)}$	Mass erase time	T_A = -40°C ~ +125 °C	—	18.06	—	ms
$t_{MERASE(384K)}$	Mass erase time	T_A = -40°C ~ +125 °C	146	—	2578	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.11. NRST pin characteristics

Table 4-18. NRST pin characteristics

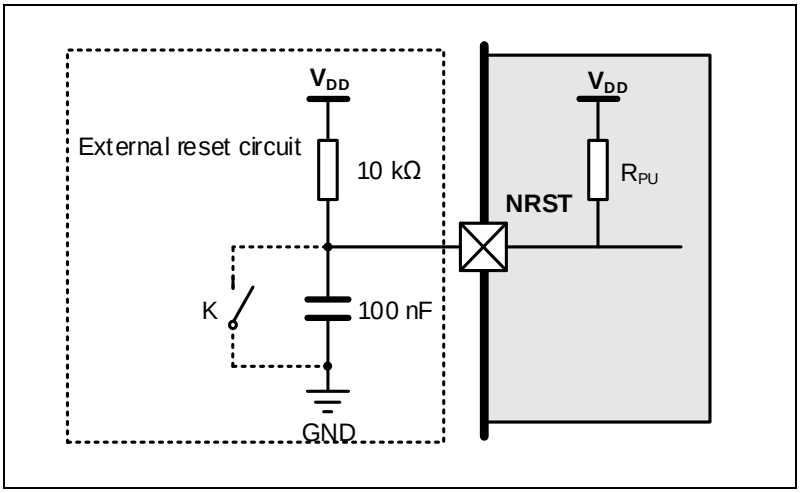
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 2.7 V	-0.3	—	0.35 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.3	

V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	380	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 5 V	-0.3	—	0.35 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	570	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 5.5 V	-0.3	—	0.35 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	610	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.12. GPIO characteristics

Table 4-19. I/O port DC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	All IO Pins Low level input voltage	2.7 V ≤ V_{DD} = V_{DDA} ≤ 5.5 V	—	—	0.3 V_{DD}	V
V_{IH}	All IO Pins High level input voltage	2.7 V ≤ V_{DD} = V_{DDA} ≤ 5.5 V	0.7 V_{DD}	—	—	
IO_speed=50MHz						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	—	0.16	—	V
		V_{DD} = 5 V	—	0.10	—	
		V_{DD} = 5.5 V	—	0.09	—	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.7 V	—	0.44	—	
		V_{DD} = 5 V	—	0.25	—	
		V_{DD} = 5.5 V	—	0.24	—	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	—	2.51	—	
		V_{DD} = 5 V	—	4.87	—	
		V_{DD} = 5.5 V	—	5.37	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.7 V	—	2.16	—	
		V_{DD} = 5 V	—	4.67	—	
		V_{DD} = 5.5 V	—	5.19	—	
IO_speed=10MHz						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	—	0.26	—	V
		V_{DD} = 5 V	—	0.18	—	
		V_{DD} = 5.5 V	—	0.17	—	
	(I_{IO} = +12 mA)	V_{DD} = 2.7 V	—	0.69	—	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 5 V	—	0.60	—	
		V_{DD} = 5.5 V	—	0.56	—	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	—	2.38	—	
		V_{DD} = 5 V	—	4.79	—	
		V_{DD} = 5.5 V	—	5.30	—	
	(I_{IO} = +12 mA)	V_{DD} = 2.7 V		1.86		
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 5 V	—	4.23	—	
		V_{DD} = 5.5 V	—	4.78	—	
IO_speed=2MHz						
V_O	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.7 V	—	0.12	—	V
		V_{DD} = 5 V		0.07		
		V_{DD} = 5.5 V		0.06		
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.7 V	—	0.52	—	
		V_{DD} = 5 V		0.27		
		V_{DD} = 5.5 V	—	0.26	—	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.7 V	—	2.50	—	
		V_{DD} = 5 V		4.87		
		V_{DD} = 5.5 V		5.38		
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.7 V	—	1.69	—	
		V_{DD} = 5 V		4.50		
		V_{DD} = 5.5 V	—	5.02	—	
R_{PU}(2)	Internal pull-up resistor	—	—	40	—	kΩ
R_{PD}(2)	Internal pull-down resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-20. I/O port AC characteristics(1)(2)(4)

GPIOx_OSPD[1:0] bit value(3)	Parameter	Conditions	Typ	Unit
GPIOx_OSPD->OSPDy[1:0] = X0 （IO_Speed = 2 MHz）	T_{Rise}/T_{Fall}	2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 10 pF	50.4	ns
		2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF	61.2	

GPIOx_OSPD[1:0] bit value(3)	Parameter	Conditions	Typ	Unit
		2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 50 pF	71.2	
GPIOx_OSPD->OSPDy[1:0] = 01 （IO_Speed = 10 MHz）	T_{Rise}/T_{Fall}	2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 10 pF	11.6	ns
		2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF	14.8	
		2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 50 pF	16.4	
GPIOx_OSPD->OSPDy[1:0] = 11 （IO_Speed = 50 MHz）	T_{Rise}/T_{Fall}	2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 10 pF	2.8	ns
		2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF	3.6	
		2.7 ≤ V_{DD} ≤ 5.5 V, C_L = 50 pF	4.4	

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all test results given for T_A = 25 °C.
(3) The I/O speed is configured using the GPIOx_OSPD -> OSPDy[1:0] bits.
(4) Only for reference, Depending on user's design.

4.13. ADC characteristics

Table 4-21. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.7	5.0	5.5	V
V_{REFP}(2) (3)	Positive Reference Voltage	—	2.7	5.0	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{REFP}	V
V_{REFINT}	Internal Reference Voltage	T_J=-40℃~150℃	1.16	1.2	1.24	V
f_{ADC}(1)	ADC clock	—	0.1	—	15	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	1	MSPs
		10-bit	0.008	—	1.15	
		8-bit	0.009	—	1.36	
		6-bit	0.011	—	1.67	
V_{AIN}(1)	Analog input voltage	32 external, 2 internal	0	—	V_{REFP}	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	823	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	500	Ω
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	9	pF
t_s(2)	Sampling time	f_{ADC} = 15 MHz	0.17	—	32	μs
			2.5	—	479.5	$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	12-bit	—	15	—	$1/ f_{ADC}$
		10-bit	—	13	—	
		8-bit	—	11	—	
		6-bit	—	9	—	
t_{SU}(2)	Startup time	—	—	—	1	μs
I_{VDDA}(1)	ADC consumption from the V_{DDA} supply	f_{ADC} = 15 MHz, V_{DDA} = V_{REF+} = 5 V	—	1	—	mA
I_{VDD}(1)	ADC consumption from the V_{DD} supply	f_{ADC} = 15 MHz, V_{DDA} = V_{REF+} = 5 V	—	0.8	—	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.7	5.0	5.5	V
V_{REFP}(2) (3)	Positive Reference Voltage	—	2.7	5.0	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{REFP}	V
I_{VREF+}(1)	ADC consumption from the V_{REF+} supply	f_{ADC} = 15 MHz, V_{DDA} = V_{REF+} = 5 V	—	0.1	—	mA

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Equation 1: R_{AIN} max formula $$R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-22. ADC RAIN max for f_{ADC} = 15 MHz(2)

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
2.5	0.17	1.4
14.5	0.97	10.5
27.5	1.83	20.5
55.5	3.7	41.8
83.5	5.57	63.2
111.5	7.43	84.6
143.5	9.57	109
479.5	31.97	365.5

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-23. ADC dynamic accuracy at f_{ADC} = 15 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 15 MHz	—	11.1	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REFP} = 5.0 V	—	68.6	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	71.27	—	
THD	Total harmonic distortion	Temperature = 25 °C	—	-81.1	—	

(1) Based on characterization, not tested in production.

Table 4-24. ADC dynamic accuracy at f_{ADC} = 15 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 15 MHz	—	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REFP} = 2.7 V	—	66.8	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	67.2	—	
THD	Total harmonic distortion	Temperature = 25 °C	—	-79.1	—	

(1) Based on characterization, not tested in production.

Table 4-25. ADC static accuracy at f_{ADC} = 15 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 15 MHz	±3	—	LSB
DNL	Differential linearity error	V_{DDA} = V_{REFP} = 5.0 V	±3	—	
INL	Integral linearity error	Temperature = 25 °C	±5	—	

(1) Based on characterization, not tested in production.

Table 4-26. ADC static accuracy at f_{ADC} = 15 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 15 MHz	±1	—	LSB
DNL	Differential linearity error	V_{DDA} = V_{REFP} = 2.7 V	+2/-1	—	
INL	Integral linearity error	Temperature = 25 °C	±3	—	

(1) Based on characterization, not tested in production.

4.14. DAC characteristics

Table 4-27. DAC characteristics(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.7	5	5.5	V
V_{REFP}(2)	Positive Reference Voltage	—	2.7	—	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
R_{LOAD}(2)	Resistive load	Resistive load with buffer ON	1	—	—	kΩ
Ro(2)	Impedance output	Impedance output with buffer OFF	—	—	35	kΩ
C_{LOAD}(2)	Capacitive load	Capacitive load with buffer ON	—	—	100	pF
DAC_OUT min(2)	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	—	—	V
		Lower DAC_OUT voltage with buffer OFF	0.5	—	—	mV
DAC_OUT max(2)	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	—	—	V_{DDA}-0.2	V
		Higher DAC_OUT voltage with buffer OFF	—	—	V_{DDA}-1LSB	V
I_{DDA}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 5.5 V	—	590	—	μA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 5.5 V	—	670	—	
$I_{DDVREF+}$(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 5.5 V	—	95	—	μA

		With no load, worst code(0xF1C) on the input, V_{REF+} = 5.5 V	—	250	—	
DNL(1)	Differential non linearity	10-bit configuration, buffer ON	—	—	±1	LSB
		12-bit configuration, buffer ON	—	—	±4	
INL(1)	Integral non linearity	10-bit configuration, buffer ON	—	—	±1.5	LSB
		12-bit configuration, buffer ON	—	—	±6	
Offset(1)	Offset error	DAC in 12-bit mode	—	—	±22	LSB
GE(1)	Gain error	DAC in 12-bit mode, buffer ON	—	—	±1	%
$T_{setting}$(1)	Settling time	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	—	0.5	1	μs
T_{wakeup}(2)	Wakeup from off state	—	—	5	10	μs
Update rate(2)	Max frequency for a correct DAC_OUT change from code i to i±1LSB	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	—	—	2	MS/s
PSRR(2)	Power supply rejection ratio(to V_{DDA})	No R_{Load}, C_{LOAD} = 50 pF	—	-80	-55	dB

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) Buffer ON mode is recommended when using DAC at high temperature.

4.15. I2C characteristics

Table 4-28. I2C characteristics(1)(2)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The external device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-5. I2C bus timing diagram

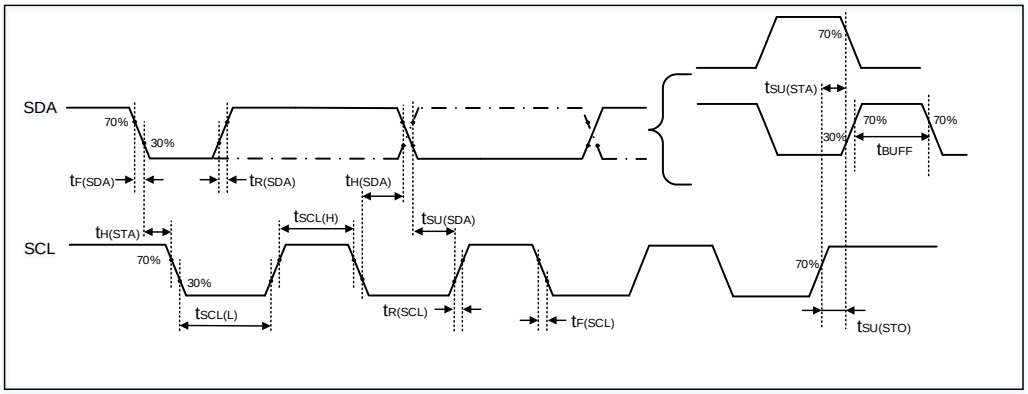


Table 4-29. I2C analog filter delay characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{AF}	Analog filter delay time	—	50	80	160	ns

(1) Guaranteed by design, not tested in production.

4.16. SPI characteristics

Table 4-30. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	V_{DD} = V_{DDA} = 5 V	—	—	22.5	MHz
$t_{sck(H)}$	SCK clock high time		—	22.22	—	ns
$t_{sck\ (L)}$	SCK clock low time		—	22.22	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	V_{DD} = V_{DDA} = 5 V	—	—	7	ns
$t_{SU(MI)}$	Data input setup time		2	—	—	ns
$t_{H(MI)}$	Data input hold time		0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	V_{DD} = V_{DDA} = 5 V, f_{PCLK} = 100 MHz	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time		2	—	—	ns
$t_{A(SO)}$	Data output access time		—	6	—	ns
$t_{DIS(SO)}$	Data output disable time	V_{DD} = V_{DDA} = 5 V	—	9	—	ns
$t_{V(SO)}$	Data output valid time		—	9	—	ns
$t_{SU(SI)}$	Data input setup time		0	—	—	ns
$t_{H(SI)}$	Data input hold time		1	—	—	ns

(1) Based on characterization, not tested in production.

Figure 4-6. SPI timing diagram - master mode

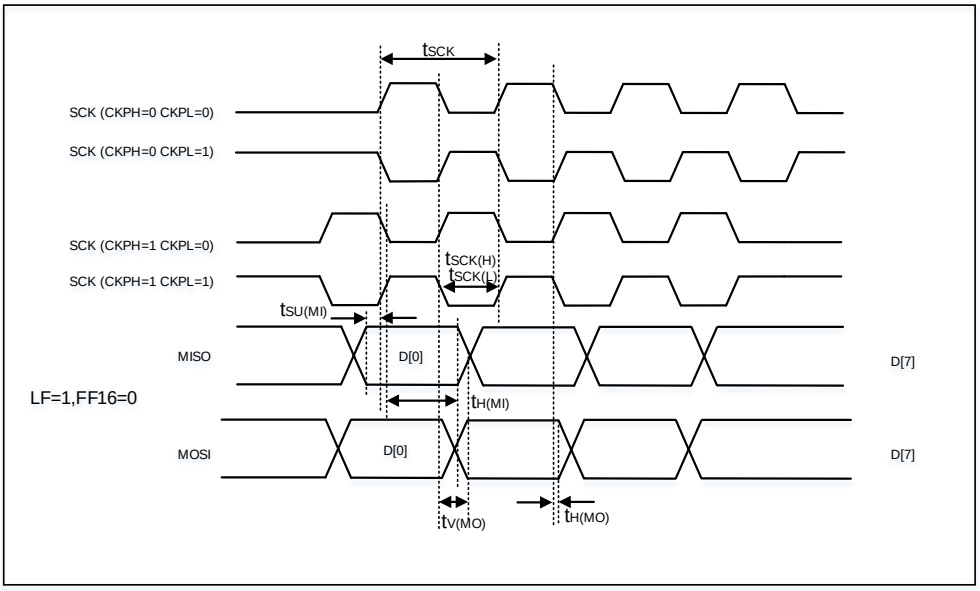
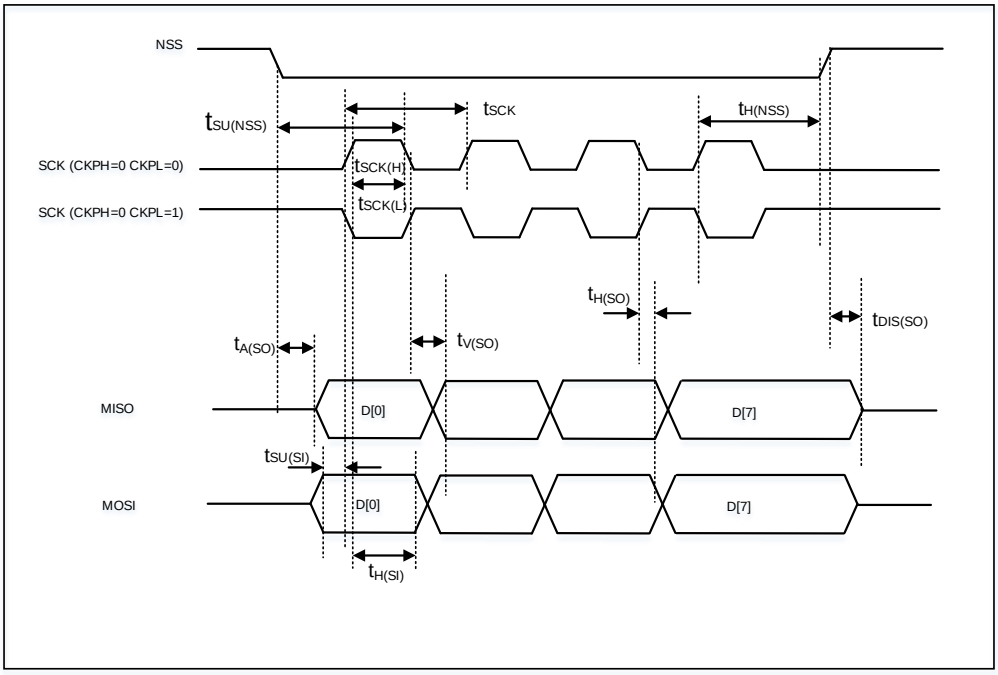


Figure 4-7. SPI timing diagram - slave mode



4.17. I2S characteristics

Table 4-31. I2S characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz
		Slave mode	—	—	12.5	
t_H	Clock high time	f_{CK}= 6.25 MHz	—	80	—	ns
t_L	Clock low time		—	80	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	1	—	—	ns
$t_{SU(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	1	—	—	ns
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	10	ns
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3	—	—	ns
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	10	ns
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

Figure 4-8. I2S timing diagram - master mode

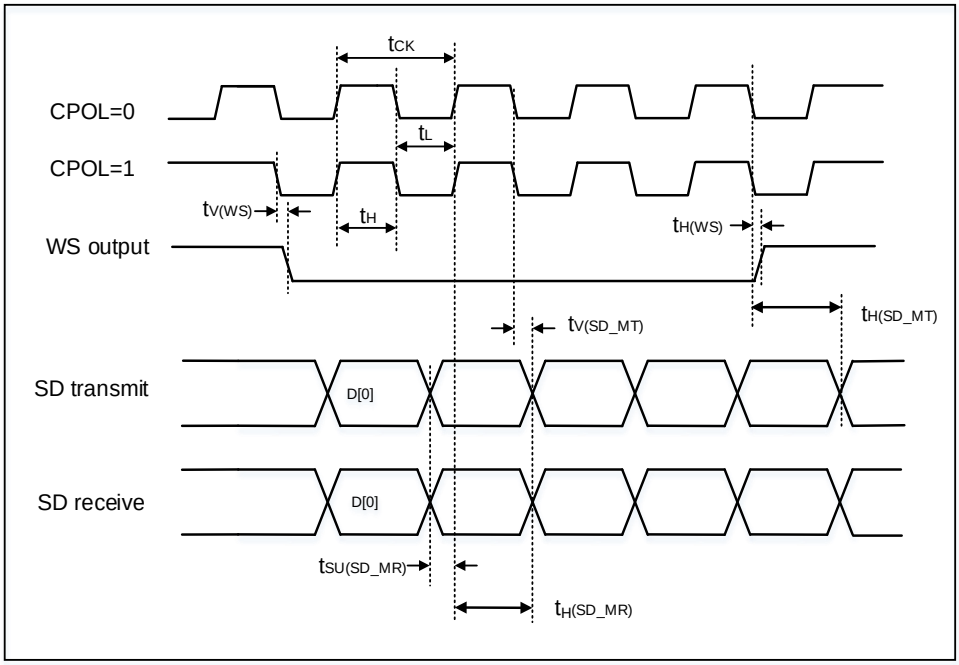
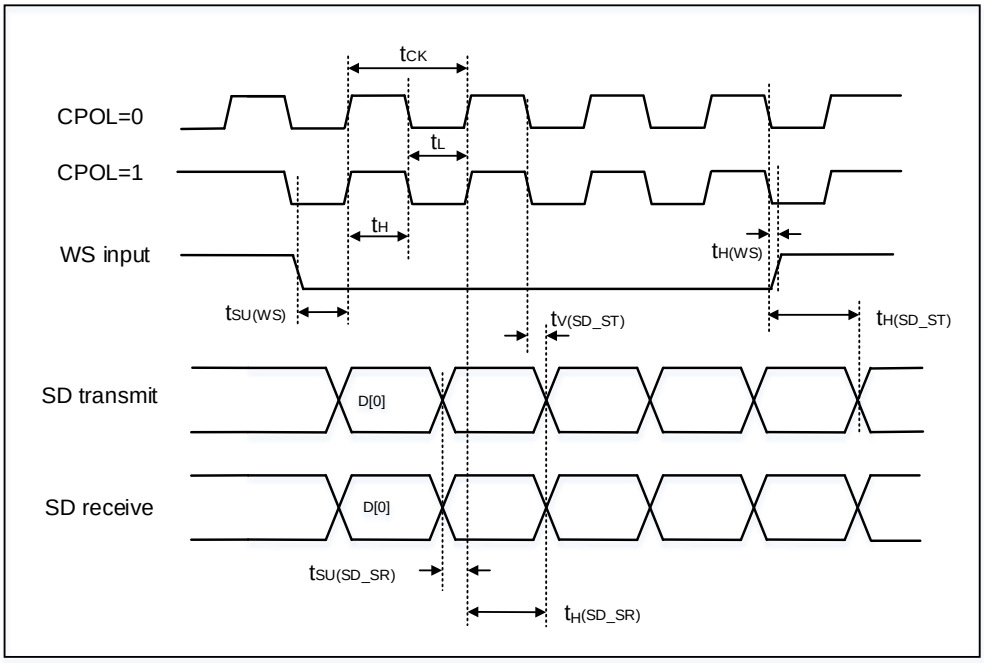


Figure 4-9. I2S timing diagram - slave mode



4.18. USART characteristics

Table 4-32. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 100 MHz	—	—	12.5	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 100 MHz	40	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 100 MHz	40	—	—	ns

(1) Guaranteed by design, not tested in production.

4.19. CAN characteristics

Refer to ***Table 4-19. I/O port DC characteristics(1)*** for more details on the input/output alternate function characteristics (CAN TX and CAN RX).

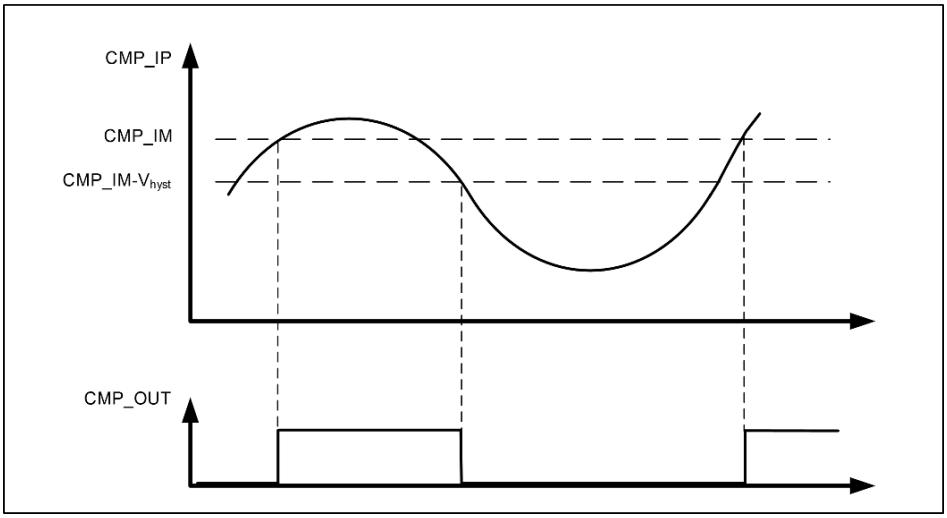
4.20. Comparators characteristics

Table 4-33. CMP characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.7	5.0	5.5	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}	V
V_{BG}	Scaler input voltage	—	—	1.2	—	V
V_{SC}	Scaler offset voltage	—	—	±5	—	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BEN = 0 (bridge disable)	—	750	—	nA
		BEN = 1 (bridge enable)	—	1.95	—	μA
t_{START_SCALER}	Scaler startup time	—	—	100	—	μs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	low power mode	—	320	—	ns
		Medium power mode	—	150	—	ns
		High speed power mode	—	50	—	ns
I_{DD}	Current consumption	low power mode	—	2.7	—	μA
		Medium power mode	—	8.2	—	
		High speed power mode	—	56	—	
V_{offset}	Offset error	—	—	±5	—	mV
V_{hyst}	Hysteresis Voltage	No Hysteresis	—	0	—	mV
		Low Hysteresis	—	18	—	
		Medium Hysteresis	—	36	—	
		High Hysteresis	—	54	—	

(1) Guaranteed by design, not tested in production.

Figure 4-10. CMP hysteresis



4.21. Temperature sensor characteristics

Table 4-34. Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{30}(1)	Uncalibrated Offset	T_A = 30°C	—	1405.6	—	mV
E_{OFF}(1)	Uncalibrated Offset Error	T_A = 30°C	—	3.3	—	mV
Avg_Slope (1)	Average slope	—	—	4.58	—	mV/°C
E_M(1)	Slope Error	—	—	60	—	μV/°C
LIN(3)	Linearity	T_A = -40 °C to 125 °C	—	-2 to2.5	—	°C
t_{s_temp}	ADC sampling time when reading the temperature	—	10	—	—	μs
t_{ON}(1)	Turn-on Time	f_{ADC} = 5 MHz, t_{s_temp} = 10 μs	—	37.8	—	μs
ETOT(2)(3)(4)	Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset	T_A = -40 °C to 125 °C	-4.5	—	5.5	°C

(1) Guaranteed by design, not tested in production.

(2) The factory-calibrated offset value is stored in the read-only area of flash in locations 0x1FFFF7F8.

(3) Based on characterization, not tested in production.

(4) The error is the average result of 100 times and represents the chip junction temperature error. The chip self-heating shall be considered when testing ambient temperature.

4.22. TIMER characteristics

Table 4-35. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 100 MHz	10	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 100 MHz	0	50	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ =100 MHz	0.01	655.36	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 100 MHz	—	42.95	s

(1) Guaranteed by design, not tested in production.

4.23. WDGT characteristics

Table 4-36. FWDGT min/max timeout period at 40 kHz (IRC40K) (1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.025	409.525	ms
1/8	001	0.025	819.025	
1/16	010	0.025	1638.025	
1/32	011	0.025	3276.025	
1/64	100	0.025	6552.025	
1/128	101	0.025	13104.025	
1/256	110 or 111	0.025	26208.025	

(1) Guaranteed by design, not tested in production.

Table 4-37. WWDGT min-max timeout value at 50 MHz (f_{PCLK1}) (1)

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	81.92	μs	5.24	ms
1/2	01	163.84		10.49	
1/4	10	327.68		20.97	
1/8	11	655.36		41.94	

(1) Guaranteed by design, not tested in production.

4.24. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 5 V, T_A = 25°C.

5. Package information

5.1. LQFP100 package outline dimensions

Figure 5-1. LQFP100 package outline

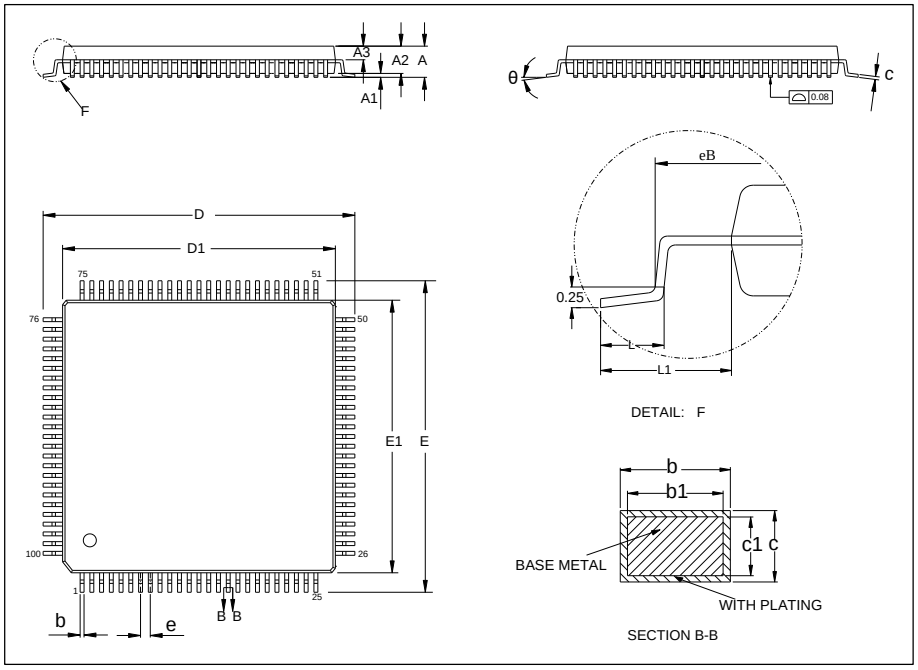
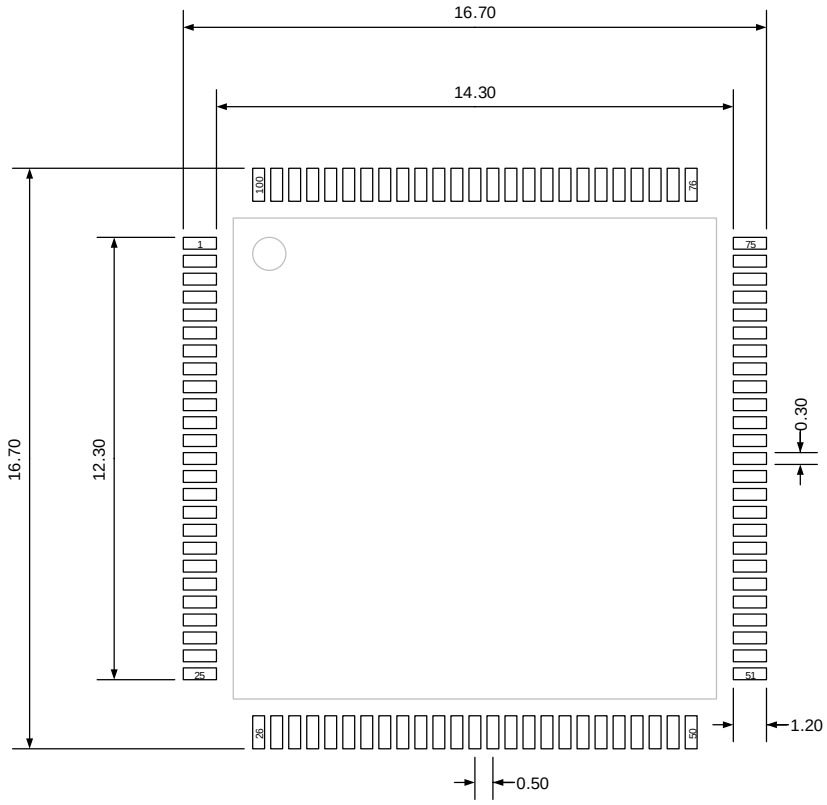


Table 5-1. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	—	0.50	—
eB	15.05	—	15.35
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-2. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.2. LQFP64 package outline dimensions

Figure 5-3. LQFP64 package outline

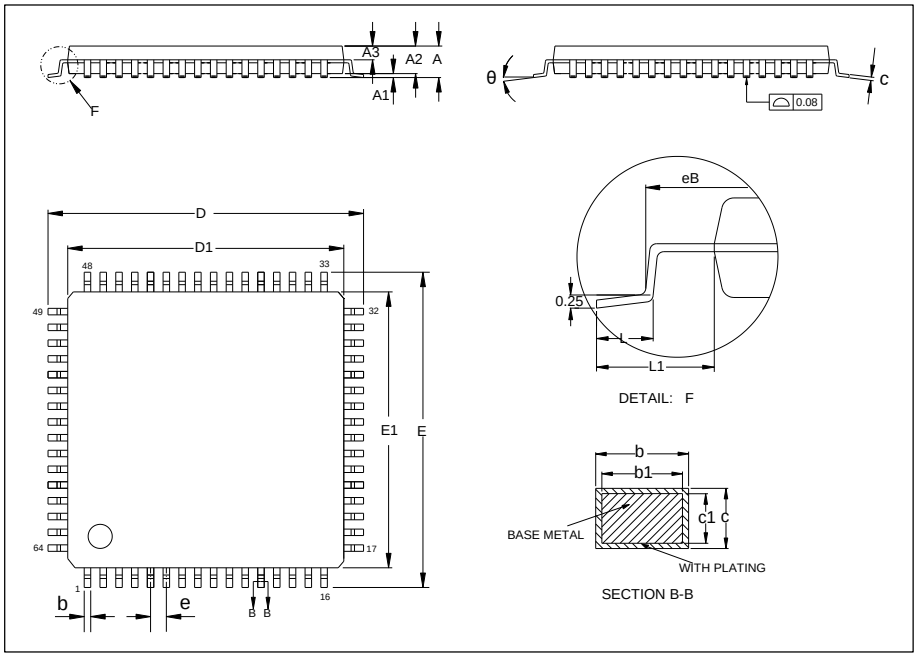
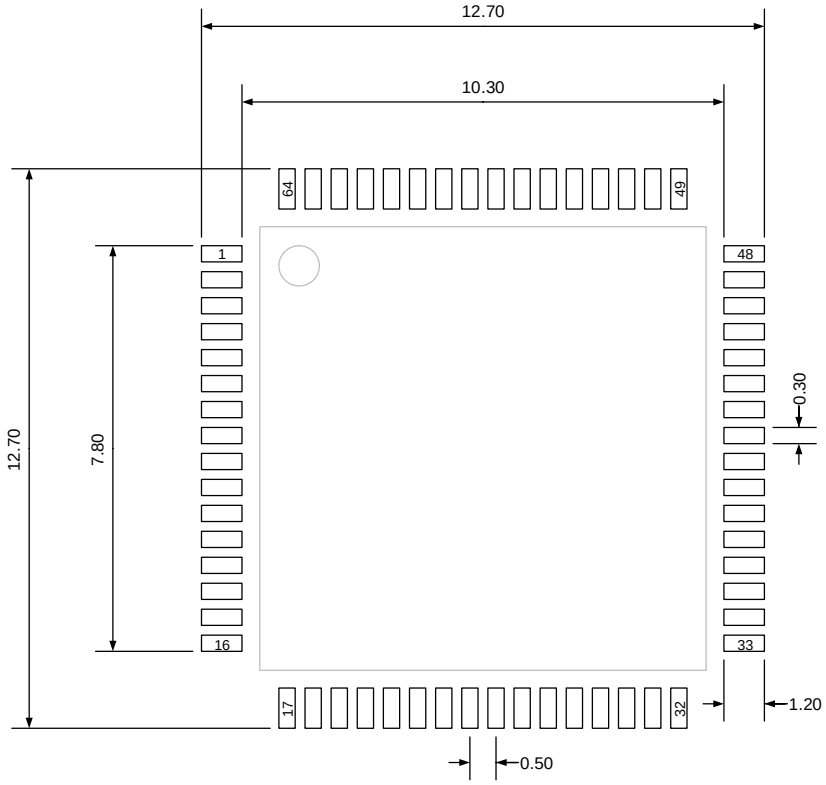


Table 5-2. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-4. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.3. LQFP48 package outline dimensions

Figure 5-5. LQFP48 package outline

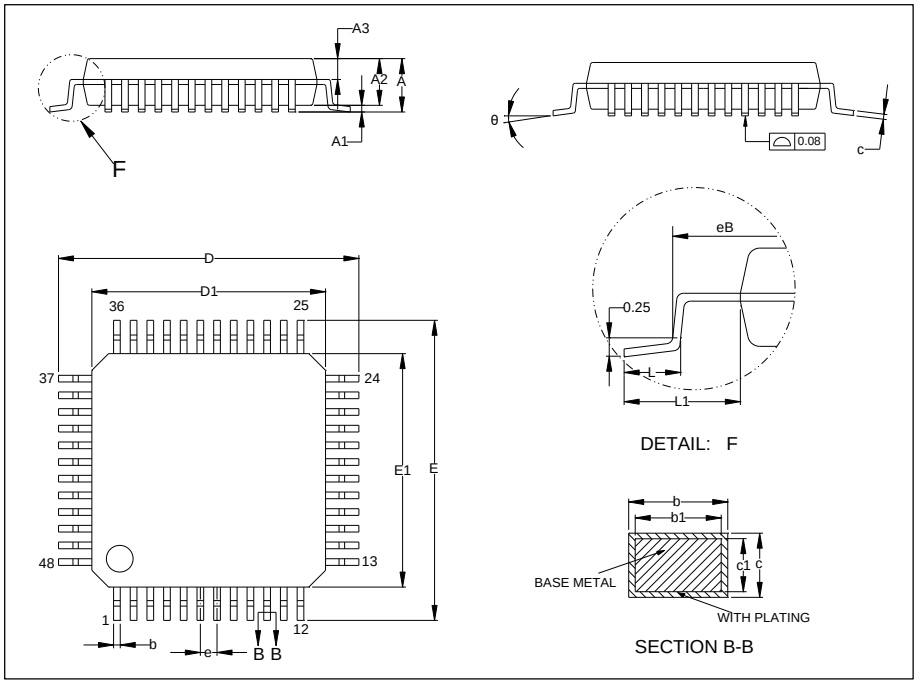
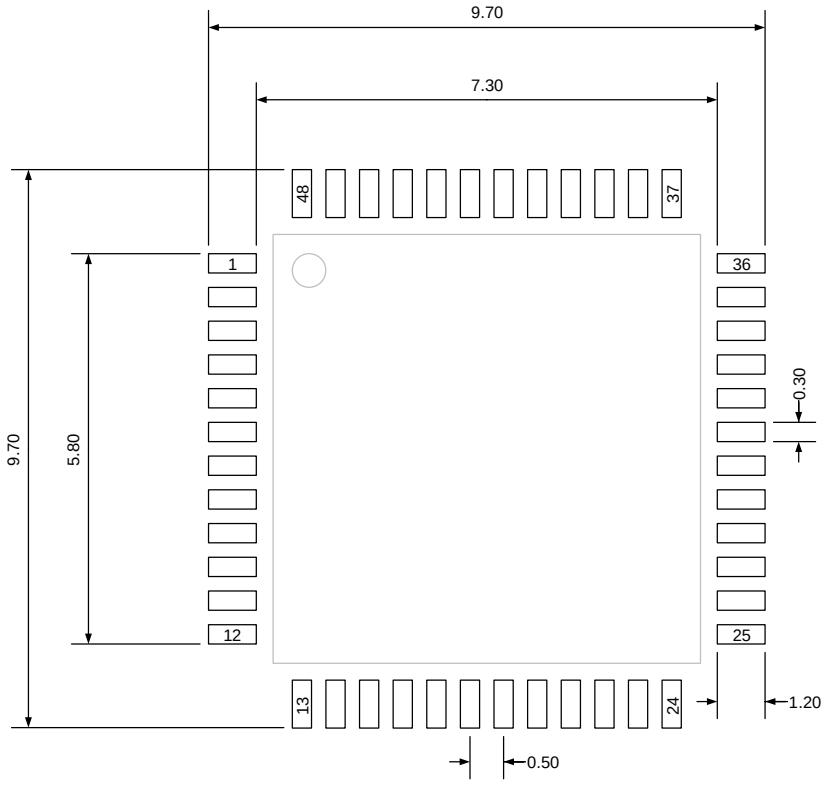


Table 5-3. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.50	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-6. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.4. QFN32 package outline dimensions

Figure 5-7. QFN32 package outline

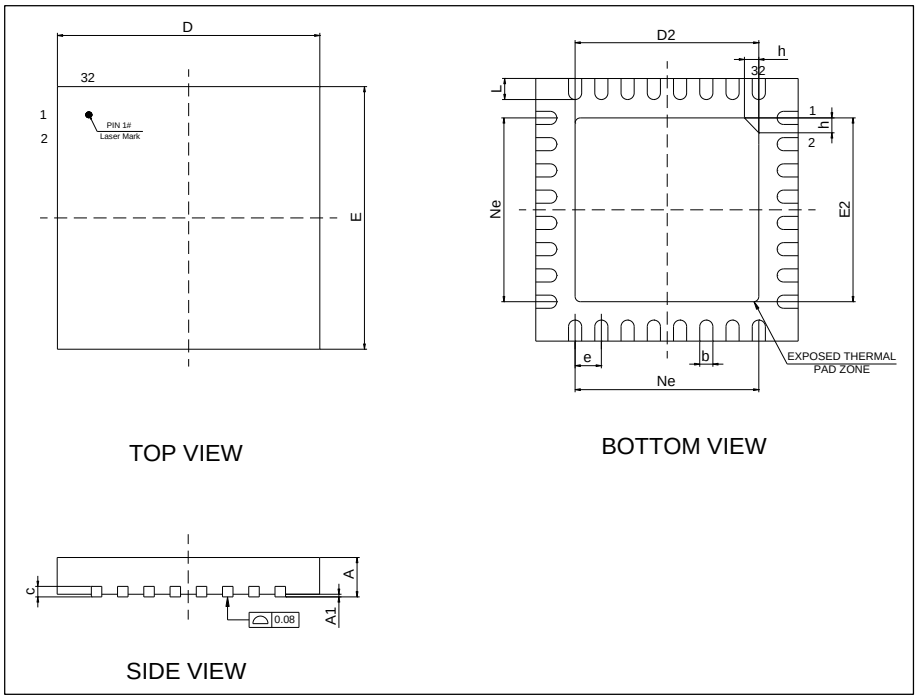
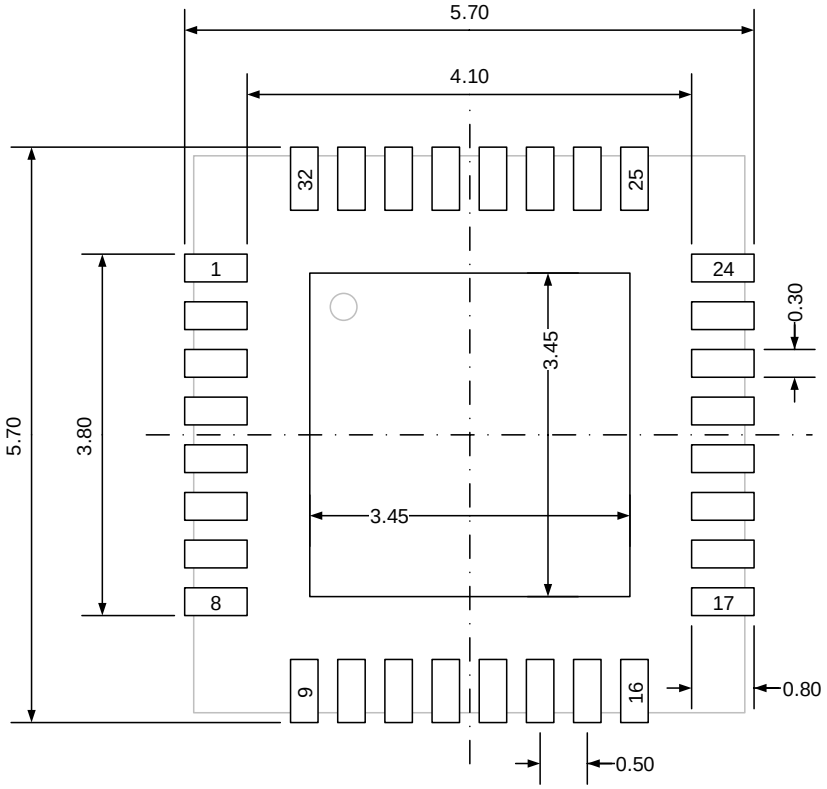


Table 5-4. QFN32 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
Ne	—	3.50	—

(Original dimensions are in millimeters)

Figure 5-8. QFN32 recommended footprint



(Original dimensions are in millimeters)

5.5. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-5. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP100	56.74	°C/W
		LQFP64	51.92	
		LQFP48	51.75	
		QFN32	37.11	
θ_{JB}	Cold plate, 2S2P PCB	LQFP100	42.61	°C/W
		LQFP64	36.72	
		LQFP48	33.32	

Symbol	Condition	Package	Value	Unit
		QFN32	9.80	
θ_{JC}	Cold plate, 2S2P PCB	LQFP100	15.02	°C/W
		LQFP64	16.60	
		LQFP48	17.23	
		QFN32	16.25	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP100	43.37	°C/W
		LQFP64	35.45	
		LQFP48	31.89	
		QFN32	9.37	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP100	1.41	°C/W
		LQFP64	0.66	
		LQFP48	0.67	
		QFN32	0.43	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32A503xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32A503VDT3	384	LQFP100	Green	Automotive -40°C to +125°C
GD32A503VCT3	256	LQFP100	Green	Automotive -40°C to +125°C
GD32A503VBT3	128	LQFP100	Green	Automotive -40°C to +125°C
GD32A503RDT3	384	LQFP64	Green	Automotive -40°C to +125°C
GD32A503RCT3	256	LQFP64	Green	Automotive -40°C to +125°C
GD32A503RBT3	128	LQFP64	Green	Automotive -40°C to +125°C
GD32A503CCT3	256	LQFP48	Green	Automotive -40°C to +125°C
GD32A503CBT3	128	LQFP48	Green	Automotive -40°C to +125°C
GD32A503KCU3	256	QFN32	Green	Automotive -40°C to +125°C
GD32A503KBU3	128	QFN32	Green	Automotive -40°C to +125°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Sep.15, 2021
1.1	1. Change SPI1 to SPI0 for quad-SPI support, refers to chapter ***Serial peripheral interface (SPI)***.	Sep.28, 2022
1.2	1. Modify written error in ***Table 4-13. Low speed external user clock characteristics (LXTAL in bypass mode)***.	Oct.12, 2022
1.3	1. Modify IO Level in ***Pin definitions***.	Oct.28, 2022
1.4	1. Modify pin name in ***Pin definitions*** and ***Pinouts and pin assignment***. 2. Conditions in ***Table 4-8. EMI characteristics modification***. 3. Change conditions in ***Table 4-8. EMI characteristics***. 4. Modify ***I2C characteristics*** diagram ***Figure 4-5. I2C bus timing diagram***.	Dec.5, 2022
1.5	1. Update pin type in ***Pin definitions***.	Feb.2, 2023
1.6	1. Update Chapter 1 and Chapter 3 feature descriptions. 2. Table header adds chip type and package in ***Pin definitions***. 3. Update Deep-Sleep mode consumption in ***Table 7-2. Power consumption characteristics***	Jun.20, 2023
1.7	1. Update Chapter 4 and Chapter 5 electric parameter	Jan.5, 2024
1.8	1. Add table 4-29. 2. Update Table 4-36 parameters Same as the user manual. 3. Update package outline dimensions.	Jul.9, 2024
1.9	1. Add Safety-26262 information in ***Table 2-1. GD32A503xx devices features and peripheral list***	Oct.22, 2024.

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